ANALOG DEVICES

Ultralow Noise Drivers for Low Voltage ADCs

Data Sheet

ADA4930-1/ADA4930-2

FEATURES

Low input voltage noise: 1.2 nV/√Hz
Low common-mode output: 0.9 V on single supply
Extremely low harmonic distortion
- **−104 dBc HD2 at 10 MHz**
- **−79 dBc HD2 at 70 MHz**
- **−73 dBc HD2 at 100 MHz**
- **−101 dBc HD3 at 10 MHz**
- **−82 dBc HD3 at 70 MHz**
- **−75 dBc HD3 at 100 MHz**

High speed
- **−3 dB bandwidth of 1.35 GHz, G = 1**
- **Slew rate: 3400 V/µs, 25% to 75%**
- **0.1 dB gain flatness to 380 MHz**
- **Fast overdrive recovery of 1.5 ns**

0.5 mV typical offset voltage
Externally adjustable gain
Differential-to-differential or single-ended-to-differential operation
Adjustable output common-mode voltage
Single-supply operation: 3.3 V or 5 V

APPLICATIONS

ADC drivers
Single-ended-to-differential converters
IF and baseband gain blocks
Differential buffers
Line drivers

GENERAL DESCRIPTION

The ADA4930-1/ADA4930-2 are very low noise, low distortion, high speed differential amplifiers. They are an ideal choice for driving 1.8 V high performance ADCs with resolutions up to 14 bits from dc to 70 MHz. The adjustable output common mode allows the ADA4930-1/ADA4930-2 to match the input of the ADC. The internal common-mode feedback loop provides exceptional output balance, suppression of even-order harmonic distortion products, and dc level translation.

With the ADA4930-1/ADA4930-2, differential gain configurations are easily realized with a simple external feedback network of four resistors determining the closed-loop gain of the amplifier.

The ADA4930-1/ADA4930-2 are fabricated using Analog Devices, Inc., proprietary silicon-germanium (SiGe), complementary bipolar process, enabling them to achieve very low levels of distortion with an input voltage noise of only 1.2 nV/√Hz.

FUNCTIONAL BLOCK DIAGRAMS

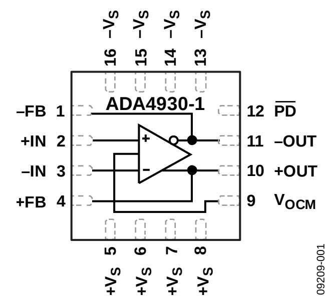

Figure 1.

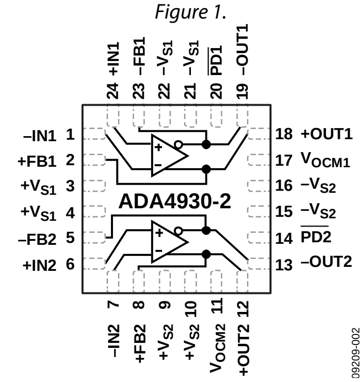

Figure 2.

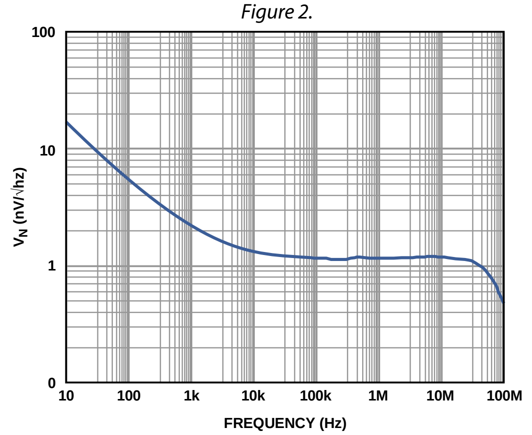

Figure 3. Voltage Noise Spectral Density

The low dc offset and excellent dynamic performance of the ADA4930-1/ADA4930-2 make them well suited for a wide variety of data acquisition and signal processing applications.

The ADA4930-1 is available in a Pb-free, 3 mm × 3 mm 16-lead LFCSP, and the ADA4930-2 is available in a Pb-free, 4 mm × 4 mm 24-lead LFCSP. The pinout has been optimized to facilitate printed circuit board (PCB) layout and minimize distortion. The ADA4930-1 is specified to operate over the −40°C to +105°C temperature range, and the ADA4930-2 is specified to operate over the −40°C to +105°C temperature range for 3.3 V or 5 V supply voltages.

Rev. D **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

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5/2017—Rev. B to Rev. C

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1/2015—Rev. A to Rev. B

Updated Outline Dimensions 25
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10/2010—Rev. 0 to Rev. A

Changes to General Description Section 1

10/2010—Revision 0: Initial Version

SPECIFICATIONS

3.3 V OPERATION

V_S = 3.3 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V, R_F = 301 Ω, R_G = 301 Ω, $R_{L,\,dm}$ = 1 kΩ, single-ended input, differential output, T_A = 25°C, T_{MIN} to T_{MAX} = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{O,\,dm}$ = 0.1 V p-p		1430		MHz
−3 dB Large Signal Bandwidth	$V_{O,\,dm}$ = 2 V p-p		887		MHz
Bandwidth for 0.1 dB Flatness	$V_{O,\,dm}$ = 0.1 V p-p				
ADA4930-1			380		MHz
ADA4930-2			89		MHz
Slew Rate	$V_{O,\,dm}$ = 2 V step, 25% to 75%		2877		V/µs
Settling Time to 0.1%	$V_{O,\,dm}$ = 2 V step, R_L = 200 Ω		6.3		ns
Overdrive Recovery Time	G = 3, $V_{IN,\,dm}$ = 0.7 V p-p pulse		1.5		ns
NOISE/HARMONIC PERFORMANCE					
HD2/HD3	$V_{O,\,dm}$ = 2 V p-p, f_C = 10 MHz		−98/−97		dB
	$V_{O,\,dm}$ = 2 V p-p, f_C = 30 MHz		−91/−88		dB
	$V_{O,\,dm}$ = 2 V p-p, f_C = 70 MHz		−79/−79		dB
	$V_{O,\,dm}$ = 2 V p-p, f_C = 100 MHz		−73/−73		dB
Third-Order IMD	$V_{O,\,dm}$ = 1 V p-p/tone, f_C = 70.05 MHz ± 0.05 MHz		91		dBc
	$V_{O,\,dm}$ = 1 V p-p/tone, f_C = 140.05 MHz ± 0.05 MHz		86		dBc
Input Voltage Noise	f = 100 kHz		1.15		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
Crosstalk	f = 100 MHz, ADA4930-2, R_L = 200 Ω		−90		dB
DC PERFORMANCE					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} = 0 V, R_L = open circuit	−3.1	−0.5	+3.1	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		2.75		µV/°C
Input Bias Current		−36	−24	−16	µA
Input Bias Current Drift	T_{MIN} to T_{MAX}		−0.05		µA/°C
Input Offset Current		−1.8	+0.1	+1.8	µA
Open-Loop Gain	R_F = R_G = 10 kΩ, ΔV_O = 0.5 V, R_L = open circuit		64		dB
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		0.3		1.2	V
Input Resistance	Differential		150		kΩ
	Common mode		3		MΩ
Input Capacitance	Common mode		1		pF
CMRR	ΔV_{ICM} = 0.5 V dc; R_F = R_G = 10 kΩ, R_L = open circuit		−82	−77	dB
OUTPUT CHARACTERISTICS					
Output Voltage	Each single-ended output; R_F = R_G = 10 kΩ	0.11		1.74	V
Linear Output Current	Each single-ended output; f = 1 MHz, TDH ≤ 60 dBc		30		mA
Output Balance Error	f = 1 MHz		55		dB

3.3 V V_{OCM} TO $V_{O, CM}$ PERFORMANCE

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		745		MHz
Slew Rate	$V_{O, cm}$ = 2 V p-p, 25% to 75%		828		V/μs
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		0.8		1.1	V
Input Resistance		7.0	8.3	10.3	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} - V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−25	+15.4	+31	mV
Input Voltage Noise	f = 100 kHz		23.5		nV/√Hz
Gain		0.99	1	1.02	V/V
CMRR	ΔV_{OCM} = 0.5 V dc; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−83	−77	dB

3.3 V GENERAL PERFORMANCE

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			3.3		V
Quiescent Current per Amplifier	Enabled	32	35	40	mA
	Enabled, T_{MIN} to T_{MAX} variation		81		μA/°C
	Disabled	0.44	1.8	2.35	mA
+PSRR	ΔV_{ICM} = 0.5 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−74	−70	dB
−PSRR	ΔV_{ICM} = 0.5 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−87	−76	dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Disabled		<0.8		V
	Enabled		>1.3		V
Turn-Off Time			1		μs
Turn-On Time			12		ns
$\overline{PD}$ Pin Bias Current					
Enabled	$\overline{PD}$ = 3.3 V		0.09		μA
Disabled	$\overline{PD}$ = 0 V		97		μA
OPERATING TEMPERATURE RANGE		−40		+105	°C

5 V OPERATION

V_S = 5 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V, R_F = 301 Ω, R_G = 301 Ω, $R_{L, dm}$ = 1 kΩ, single-ended input, differential output, T_A= 25°C, T_{MIN} to T_{MAX} = −40°C to +105°C, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{O, dm}$ = 0.1 V p-p		1350		MHz
−3 dB Large Signal Bandwidth	$V_{O, dm}$ = 2 V p-p		937		MHz
Bandwidth for 0.1 dB Flatness	$V_{O, dm}$ = 0.1 V p-p				
ADA4930-1			369		MHz
ADA4930-2			90		MHz
Slew Rate	$V_{O, dm}$ = 2 V step, 25% to 75%		3400		V/µs
Settling Time to 0.1%	$V_{O, dm}$ = 2 V step, R_L = 200 Ω		6		ns
Overdrive Recovery Time	G = 3, $V_{IN, dm}$ = 0.7 V p-p pulse		1.5		ns
NOISE/HARMONIC PERFORMANCE					
HD2/HD3	$V_{O, dm}$ = 2 V p-p, f_C = 10 MHz		−104/−101		dB
	$V_{O, dm}$ = 2 V p-p, f_C = 30 MHz		−91/−93		dB
	$V_{O, dm}$ = 2 V p-p, f_C = 70 MHz		−79/−82		dB
	$V_{O, dm}$ = 2 V p-p, f_C = 100 MHz		−73/−75		dB
Third-Order IMD	$V_{O, dm}$ = 1 V p-p/tone, f_C = 70.05 MHz ± 0.05 MHz		94		dBc
	$V_{O, dm}$ = 1 V p-p/tone, f_C = 140.05 MHz ± 0.05 MHz		90		dBc
Input Voltage Noise	f = 100 kHz		1.2		nV/√Hz
Input Current Noise	f = 100 kHz		2.8		pA/√Hz
Crosstalk	f = 100 MHz, ADA4930-2, R_L = 200 Ω		−90		dB
DC PERFORMANCE					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} = 0 V, R_L = open circuit	−3.1	−0.15	+3.1	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.8		µV/°C
Input Bias Current		−34	−23	−15	µA
Input Bias Current Drift	T_{MIN} to T_{MAX}		−0.05		µA/°C
Input Offset Current		−0.82	+0.1	+0.82	µA
Open-Loop Gain	R_F = R_G = 10 kΩ, ΔV_O = 1 V, R_L = open circuit		64		dB
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		0.3		2.8	V
Input Resistance	Differential		150		kΩ
	Common mode		3		MΩ
Input Capacitance	Common mode		1		pF
CMRR	ΔV_{ICM} = 1 V dc; R_F = R_G = 10 kΩ, R_L = open circuit		−82	−77	dB
OUTPUT CHARACTERISTICS					
Output Voltage	Each single-ended output; R_F = R_G = 10 kΩ	0.18		3.38	V
Linear Output Current	Each single-ended output; f = 1 MHz, TDH ≤ 60 dBc		30		mA
Output Balance Error	f = 1 MHz		55		dB

5 V V_{OCM} TO $V_{O, CM}$ PERFORMANCE

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	$V_{O, cm}$ = 0.1 V p-p		740		MHz
Slew Rate	$V_{O, cm}$ = 2 V p-p, 25% to 75%		1224		V/μs
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		0.5		2.3	V
Input Resistance		7.0	8.3	10.2	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{O, cm} − V_{OCM}$; $V_{IP} = V_{IN} = V_{OCM}$ = 0 V	−25	+0.35	+15	mV
Input Voltage Noise	f = 100 kHz		23.5		nV/√Hz
Gain		0.99	1	1.02	V/V
CMRR	ΔV_{OCM} = 1.5 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−80	−77	dB

5 V GENERAL PERFORMANCE

Table 6.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			5		V
Quiescent Current per Amplifier	Enabled	31.1	34	38.4	mA
	Enabled, T_{MIN} to T_{MAX} variation		74.5		μA/°C
	Disabled	0.45	1.8	2.6	mA
+PSRR	ΔV_{ICM} = 1 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−74	−71	dB
−PSRR	ΔV_{ICM} = 1 V; $R_F = R_G$ = 10 kΩ, R_L = open circuit		−91	−75	dB
POWER-DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Disabled		<2.5		V
	Enabled		>3		V
Turn-Off Time			1		μs
Turn-On Time			12		ns
$\overline{PD}$ Pin Bias Current					
Enabled	$\overline{PD}$ = 5 V		0.09		μA
Disabled	$\overline{PD}$ = 0 V		97		μA
OPERATING TEMPERATURE RANGE		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 4
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD51-7.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP (Exposed Pad)	98	°C/W
24-Lead LFCSP (Exposed Pad)	67	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4930-1/ADA4930-2 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4930-1/ADA4930-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation vs. the ambient temperature for the ADA4930-1 single 16-lead LFCSP (98°C/W) and the ADA4930-2 dual 24-lead LFCSP (67°C/W) on a JEDEC standard 4-layer board.

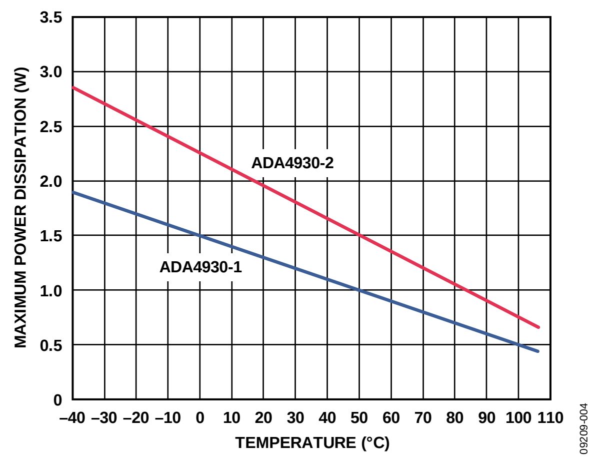


Figure 4. Maximum Power Dissipation vs. Ambient Temperature, 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

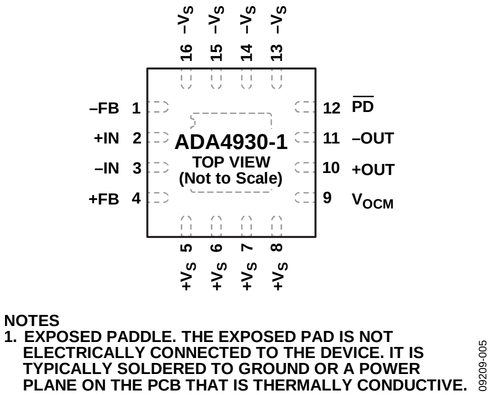


Figure 5. ADA4930-1 Pin Configuration

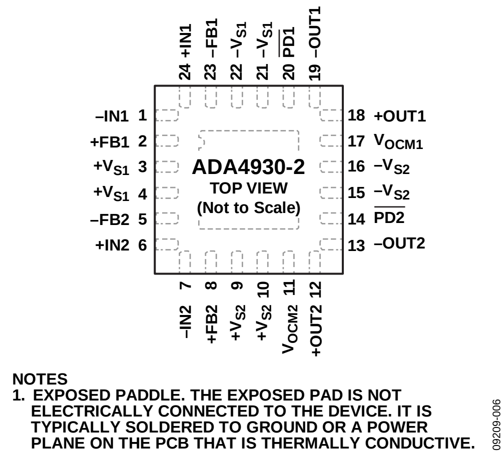


Figure 6. ADA4930-2 Pin Configuration

Table 9. ADA4930-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−FB	Negative Output for Feedback Component Connection.
2	+IN	Positive Input Summing Node.
3	−IN	Negative Input Summing Node.
4	+FB	Positive Output for Feedback Component Connection.
5 to 8	$+V_S$	Positive Supply Voltage.
9	V_{OCM}	Output Common-Mode Voltage.
10	+OUT	Positive Output for Load Connection.
11	−OUT	Negative Output for Load Connection.
12	$\overline{PD}$	Power-Down Pin.
13 to 16	$-V_S$	Negative Supply Voltage.
	EPAD	Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive.

Table 10. ADA4930-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN1	Negative Input Summing Node 1.
2	+FB1	Positive Output Feedback Pin 1.
3, 4	$+V_{S1}$	Positive Supply Voltage 1.
5	−FB2	Negative Output Feedback Pin 2.
6	+IN2	Positive Input Summing Node 2.
7	−IN2	Negative Input Summing Node 2.
8	+FB2	Positive Output Feedback Pin 2.
9, 10	$+V_{S2}$	Positive Supply Voltage 2.
11	V_{OCM2}	Output Common-Mode Voltage 2.
12	+OUT2	Positive Output 2.
13	−OUT2	Negative Output 2.
14	$\overline{PD2}$	Power-Down Pin 2.
15, 16	$-V_{S2}$	Negative Supply Voltage 2.
17	V_{OCM1}	Output Common-Mode Voltage 1.
18	+OUT1	Positive Output 1.
19	−OUT1	Negative Output 1.
20	$\overline{PD1}$	Power-Down Pin 1.
21, 22	$-V_{S1}$	Negative Supply Voltage 1.
23	−FB1	Negative Output Feedback Pin 1.
24	+IN1	Positive Input Summing Node 1.
	EPAD	Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 5 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V, $R_{L,\,dm}$ = 1 kΩ, unless otherwise noted.

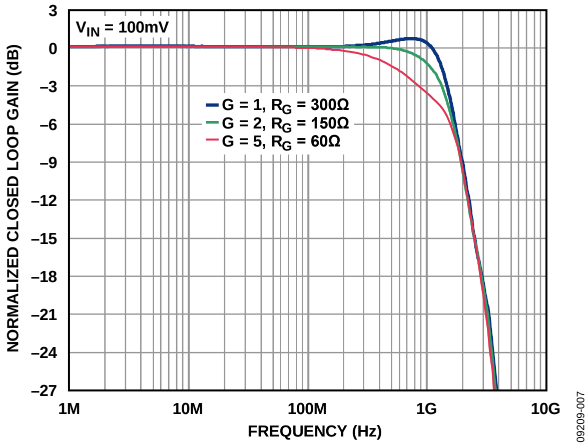


Figure 7. Small Signal Frequency Response at Gain = 1, Gain = 2, and Gain = 5

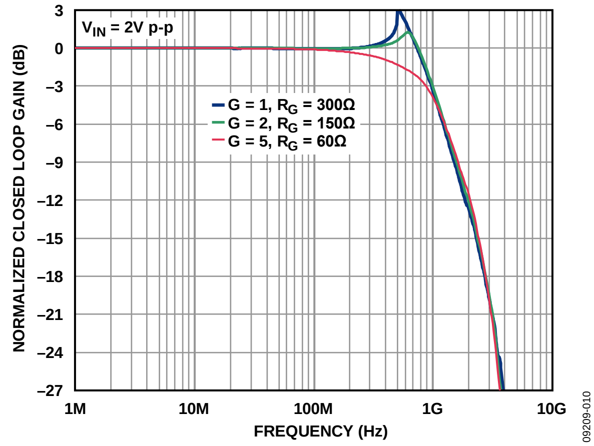


Figure 10. Large Signal Frequency Response at Gain = 1, Gain = 2, and Gain = 5

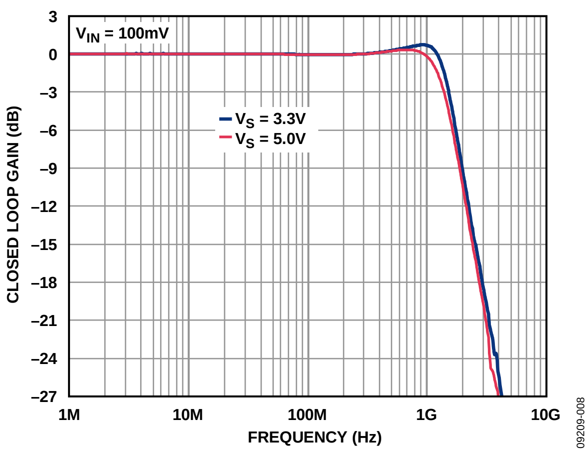


Figure 8. Small Signal Frequency Response at V_S = 3.3 V and V_S = 5 V

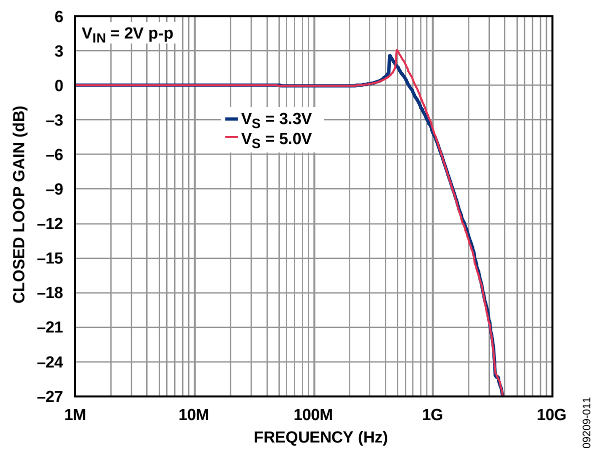


Figure 11. Large Signal Frequency Response at V_S = 3.3 V and V_S = 5 V

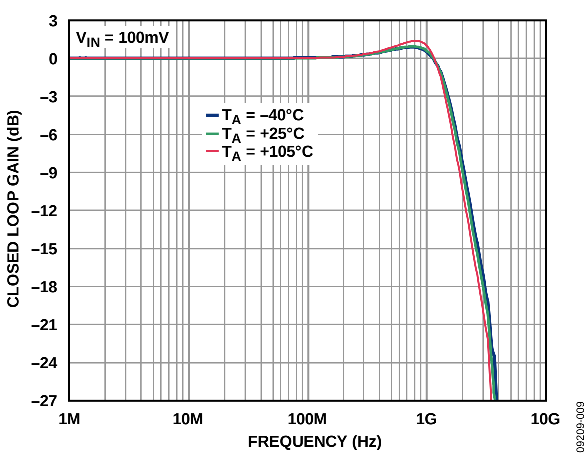


Figure 9. Small Signal Frequency Response at T_A = −40°C, T_A = 25°C, and T_A = 105°C

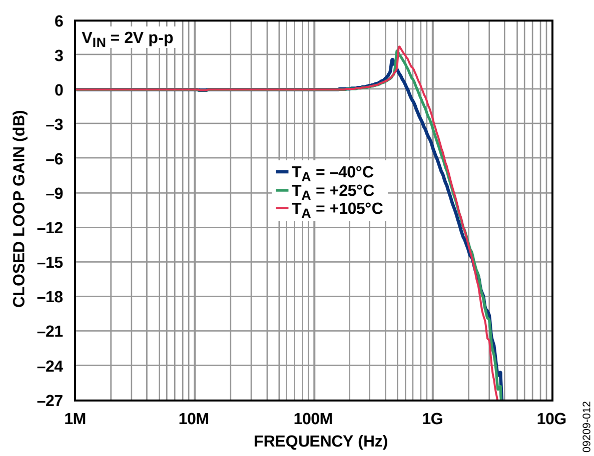


Figure 12. Large Signal Frequency Response at T_A = −40°C, T_A = 25°C, and T_A = 105°C

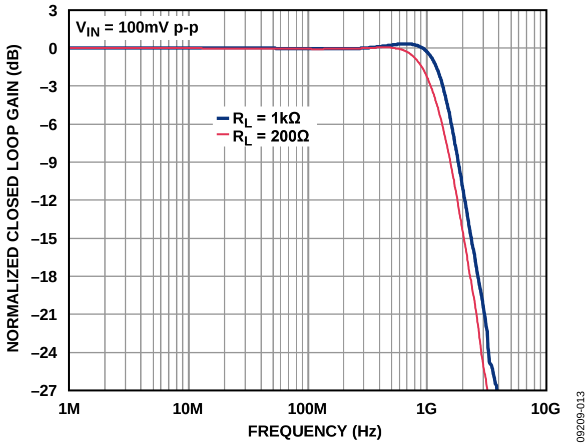


Figure 13. Small Signal Frequency Response for R_L = 200 Ω and R_L = 1 kΩ

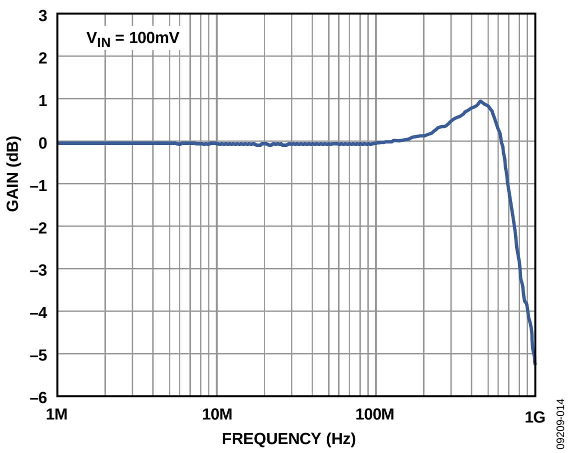


Figure 14. V_{OCM} Small Signal Frequency Response

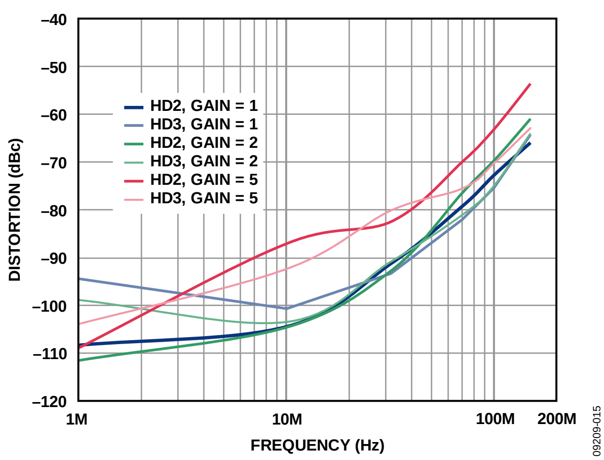


Figure 15. Harmonic Distortion vs. Frequency for Gain = 1, Gain = 2, and Gain = 5

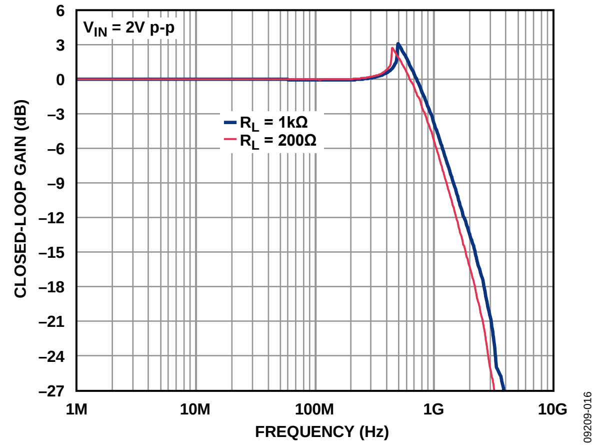


Figure 16. Large Signal Frequency Response for R_L = 200 Ω and R_L = 1 kΩ

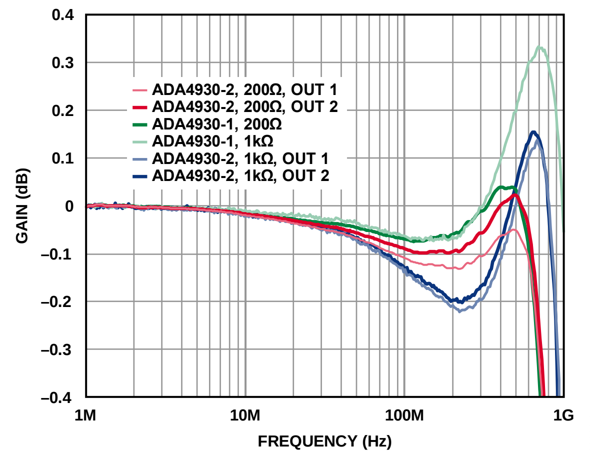


Figure 17. Small Signal 0.1 dB Flatness vs. Frequency for R_L = 200 Ω and R_L = 1 kΩ

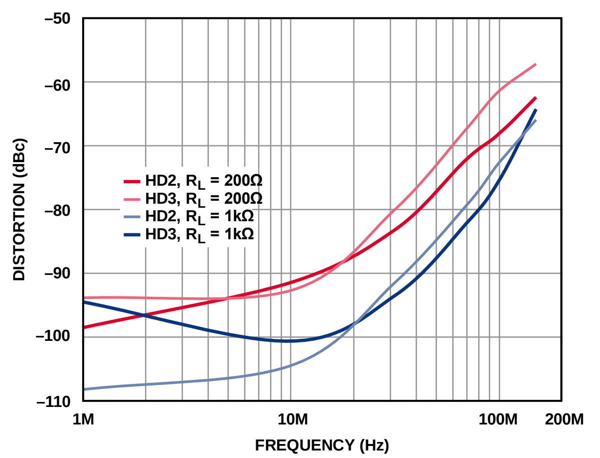


Figure 18. Harmonic Distortion vs. Frequency for R_L = 200 Ω and R_L = 1 kΩ

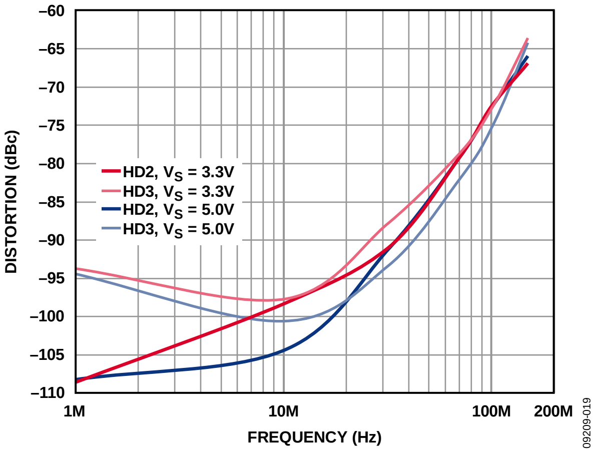


Figure 19. ADA4930-1 Harmonic Distortion vs. Frequency at V_S = 3.3 V and V_S = 5 V

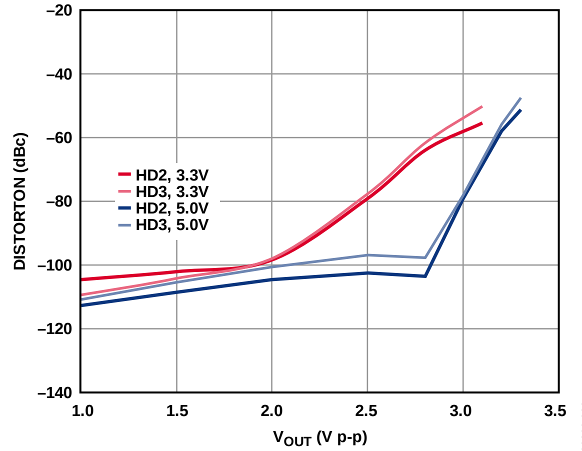


Figure 22. Harmonic Distortion vs. Output @ 10 MHz

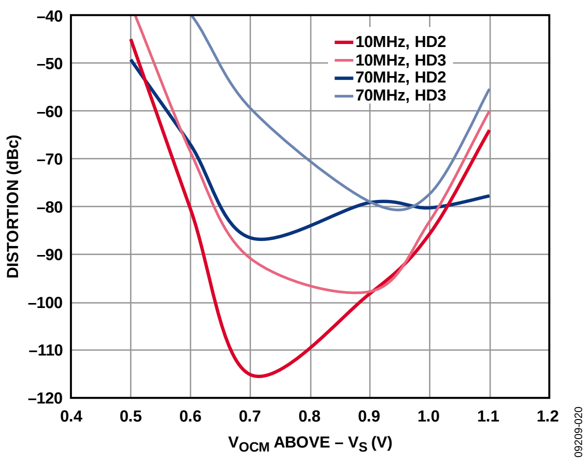


Figure 20. Harmonic Distortion vs. V_{OCM} at V_S = 3.3 V at 10 MHz and 70 MHz

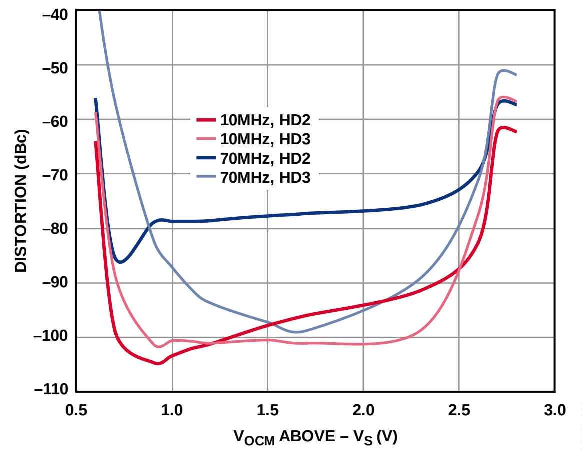


Figure 23. Harmonic Distortion vs. V_{OCM} at 10 MHz and 70 MHz

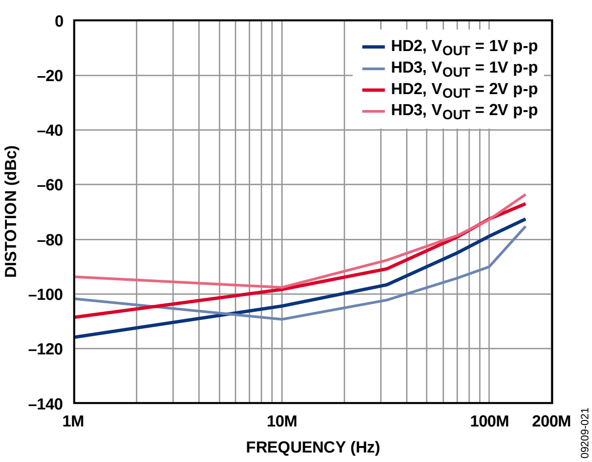


Figure 21. Distortion vs. V_{OUT} at V_S = 3.3 V

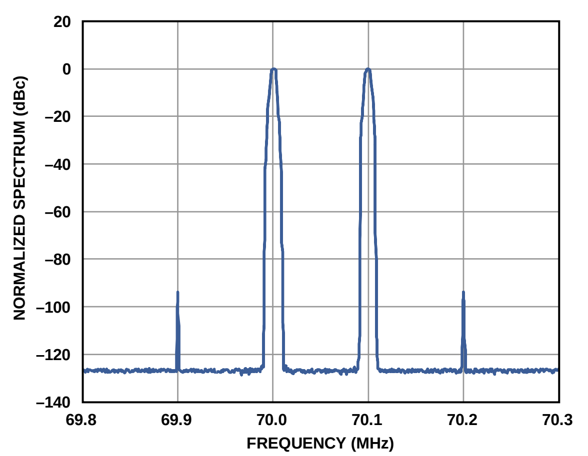


Figure 24. 70 MHz Intermodulation Distortion

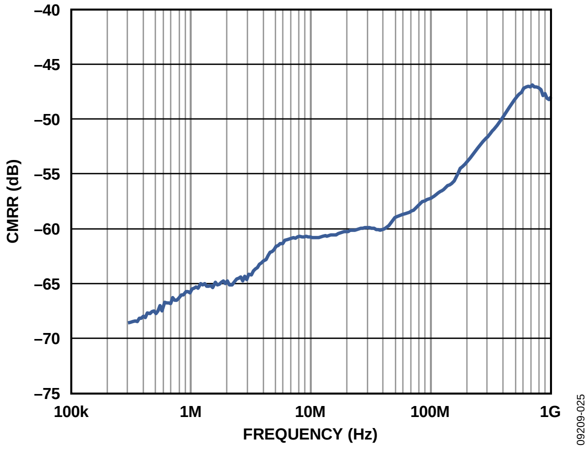


Figure 25. CMRR vs. Frequency, $R_L = 200\,\Omega$

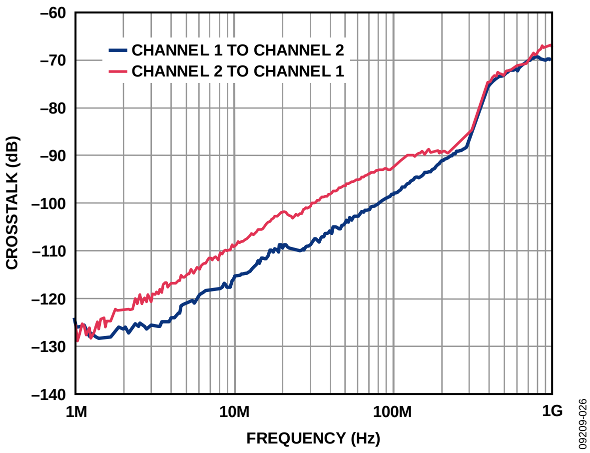


Figure 26. Crosstalk vs. Frequency, $R_L = 200\,\Omega$

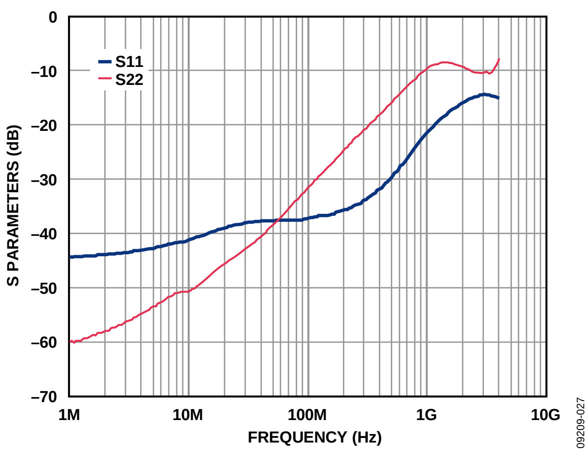


Figure 27. S11, S22, $R_L = 200\,\Omega$

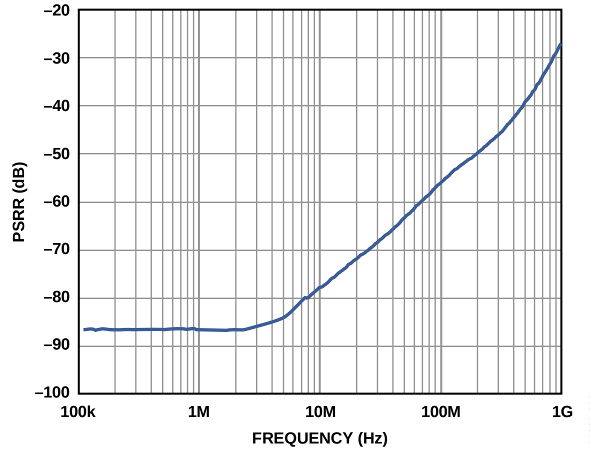


Figure 28. PSRR vs. Frequency, $R_L = 200\,\Omega$

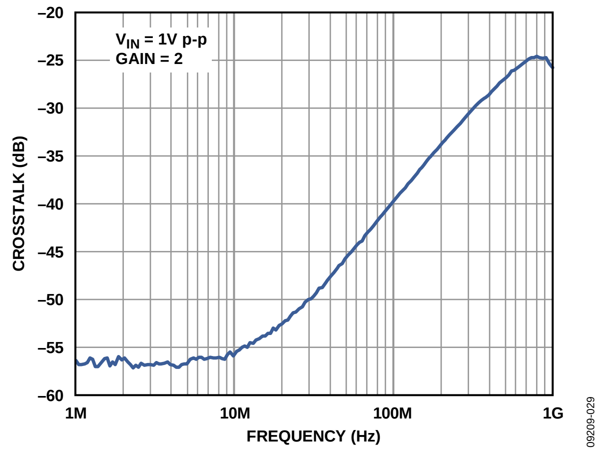


Figure 29. Output Balance vs. Frequency, $R_L = 200\,\Omega$

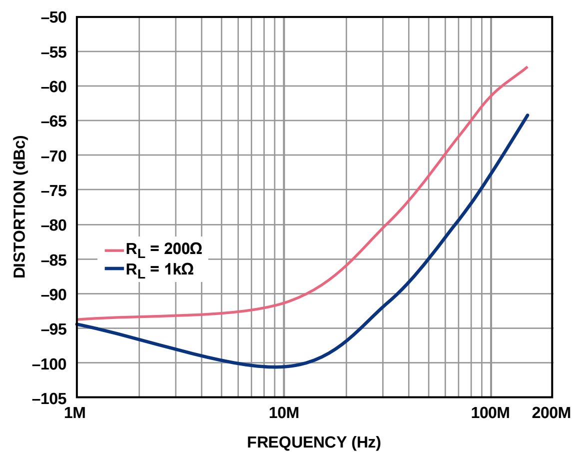


Figure 30. SFDR

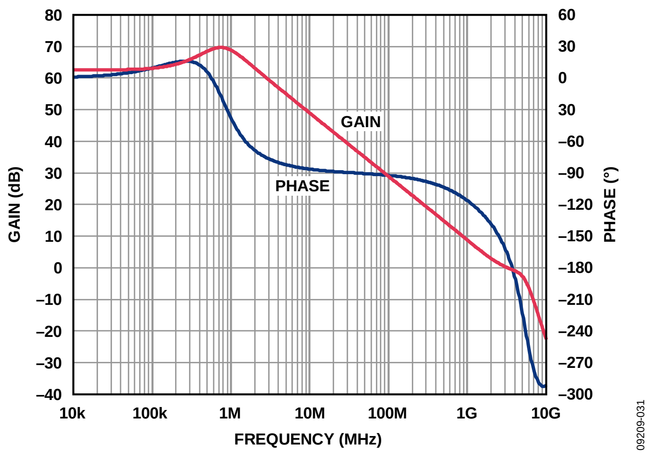


Figure 31. Open Loop Gain and Phase

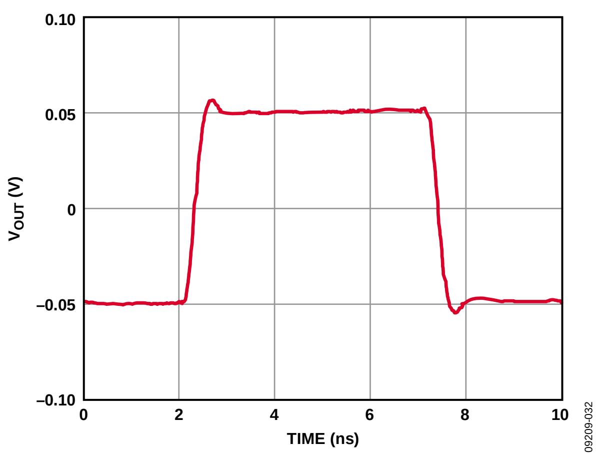


Figure 32. Small Signal Pulse Response

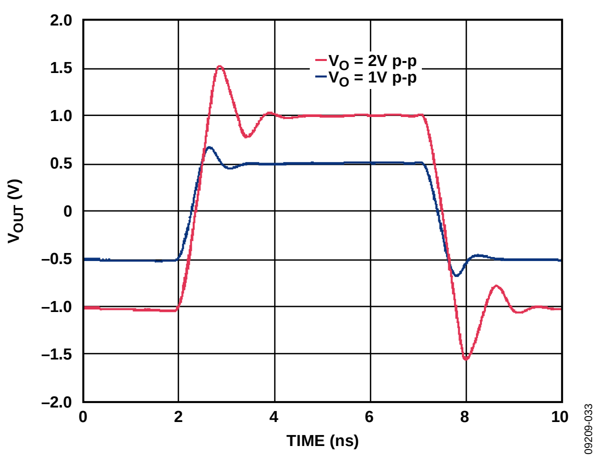


Figure 33. Large Signal Pulse Response

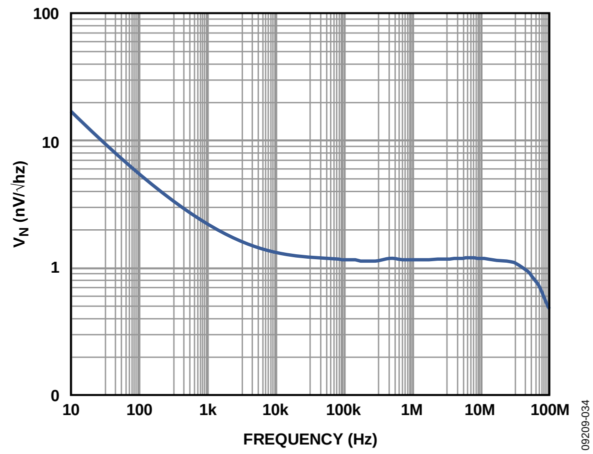


Figure 34. Voltage Noise Spectral Density

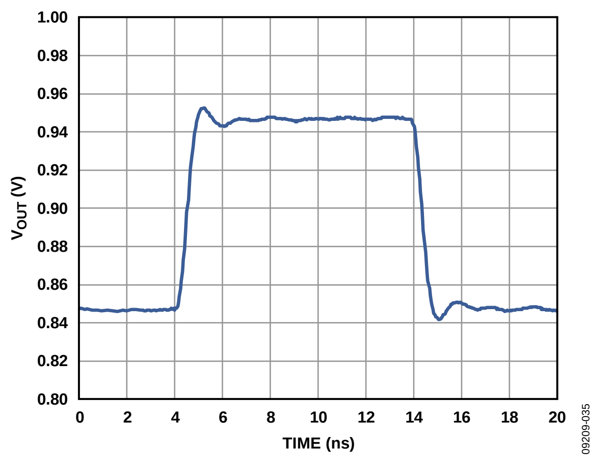


Figure 35. Small Signal V_{OCM} Pulse Response

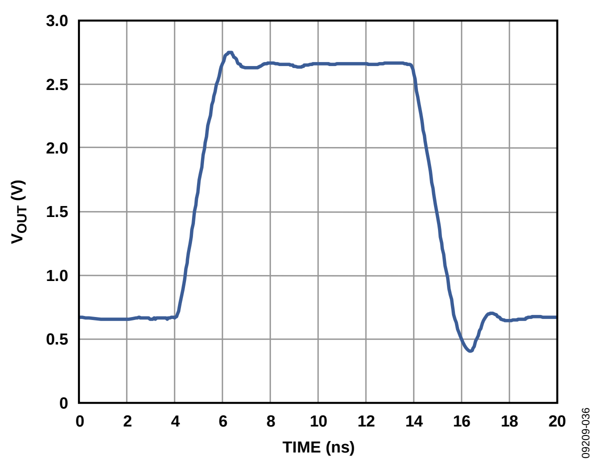


Figure 36. Large Signal V_{OCM} Pulse Response

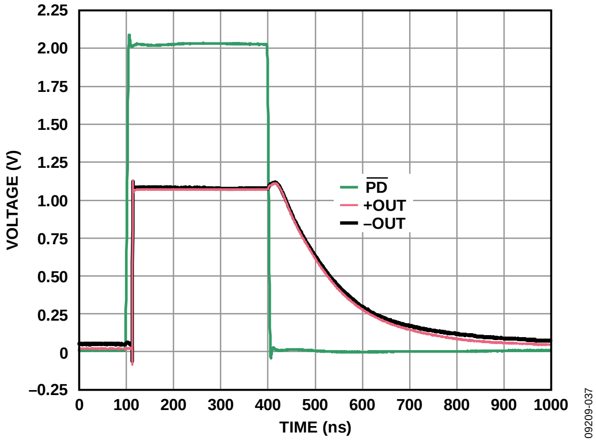


Figure 37. $\overline{PD}$ Response vs. Time

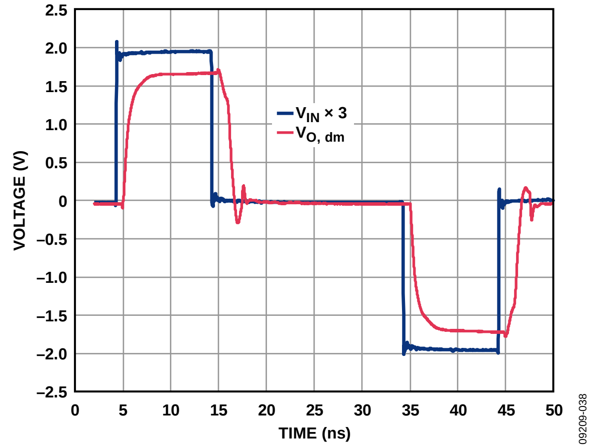


Figure 38. $V_{o,dm}$ Overdrive Recovery

TEST CIRCUITS

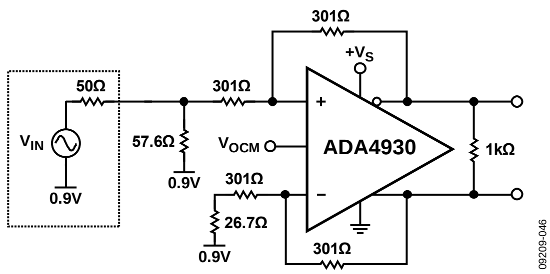


Figure 39. Equivalent Basic Test Circuit

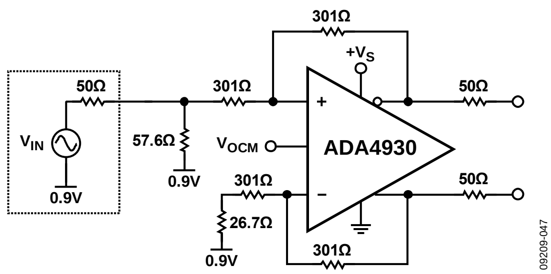


Figure 40. Test Circuit for Output Balance

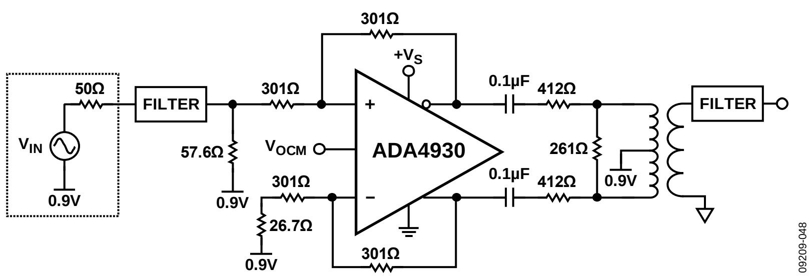


Figure 41. Test Circuit for Distortion Measurements

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

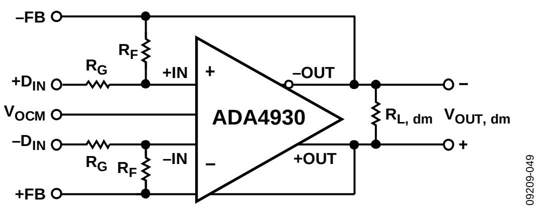


Figure 42. Circuit Definitions

Differential Voltage

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or, equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\ dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-Mode Voltage

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\ cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Output balance is a measure of how close the differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider midpoint with the magnitude of the differential signal (see Figure 39). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left|\frac{V_{OUT,\,cm}}{V_{OUT,\,dm}}\right|$$

THEORY OF OPERATION

The ADA4930-1/ADA4930-2 differ from conventional op amps in that they have two outputs whose voltages move in opposite directions and an additional input, V_{OCM}. Like an op amp, they rely on high open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4930-1/ADA4930-2 behave much like standard voltage feedback op amps and facilitate single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Like op amps, the ADA4930-1/ADA4930-2 have high input impedance and low output impedance.

Two feedback loops control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls the differential output voltage. The common-mode feedback controls the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value within the specified limits. The output common-mode voltage is forced to be equal to the voltage applied to the V_{OCM} input by the internal common-mode feedback loop.

The internal common-mode feedback loop produces outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. This results in differential outputs that are very close to the ideal of being identical in amplitude and are exactly 180° apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The ADA4930-1/ADA4930-2 use high open-loop gain and negative feedback to force their differential and common-mode output voltages to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 42). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 42 is determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

where the gain and feedback resistors, R_G and R_F, on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4930-1/ADA4930-2 can be estimated using the noise model in Figure 43. The input-referred noise voltage density, v_{nIN}, is modeled as differential. The noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground.

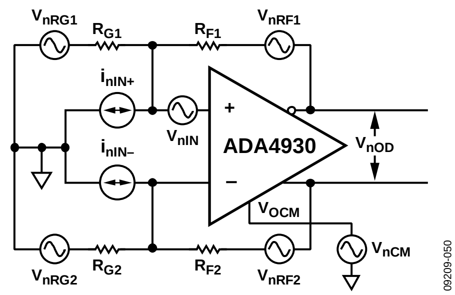


Figure 43. Noise Model

Similar to the case of conventional op amps, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by an appropriate output factor.

The output voltage due to v_{nIN} is obtained by multiplying v_{nIN} by the noise gain, G_N.

The circuit noise gain is

$$G_N = \frac{2}{(\beta_1 + \beta_2)}$$

where the feedback factors are

$$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}} \text{ and } \beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}.$$

When the feedback factors are matched, $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, $\beta 1 = \beta 2 = \beta$, and the noise gain becomes $G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$.

The noise currents are uncorrelated with the same mean-square value, and each produces an output voltage that is equal to the noise current multiplied by the associated feedback resistance.

The noise voltage density at the V_{OCM} pin is v_{nCM}. When the feedback networks have the same feedback factor, as in most cases, the output noise due to v_{nCM} is common-mode and the output noise from V_{OCM} is zero.

Each of the four resistors contributes $(4kTR_{xx})^{1/2}$. The noise from the feedback resistors appears directly at the output, and the noise from the gain resistors appears at the output multiplied by R_F/R_G.

The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} (v_{nODi})^2}$$

Table 11. Output Noise Voltage Density Calculations for Matched Feedback Networks

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Differential Output Noise Voltage Density Terms
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nOD1} = G_N(v_{nIN})$
Inverting Input	i_{nIN+}	$i_{nIN+} \times (R_{F2})$	1	$v_{nOD2} = (i_{nIN+})(R_{F2})$
Noninverting Input	i_{nIN-}	$i_{nIN-} \times (R_{F1})$	1	$v_{nOD3} = (i_{nIN-})(R_{F1})$
V_{OCM} Input	v_{nCM}	v_{nCM}	0	$v_{nOD4} = 0$
Gain Resistor R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	R_{F1}/R_{G1}	$v_{nOD5} = (R_{F1}/R_{G1})(4kTR_{G1})^{1/2}$
Gain Resistor R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	R_{F2}/R_{G2}	$v_{nOD6} = (R_{F2}/R_{G2})(4kTR_{G2})^{1/2}$
Feedback Resistor R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nOD7} = (4kTR_{F1})^{1/2}$
Feedback Resistor R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nOD8} = (4kTR_{F2})^{1/2}$

Table 12. Differential Input, DC-Coupled, V_S = 5 V

Nominal Gain (dB)	R_{F1}, R_{F2} (Ω)	R_{G1}, R_{G2} (Ω)	$R_{IN,\,dm}$ (Ω)	Differential Output Noise Density (nV/√Hz)
0	301	301	602	4.9
6	301	150	300	6.2
10	301	95.3	190.6	7.8
14	301	60.4	120.4	10.1

Table 13. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω, V_S = 5 V

Nominal Gain (dB)	R_{F1}, R_{F2} (Ω)	R_{G1} (Ω)	R_T (Ω)	$R_{IN,\,cm}$ (Ω)	R_{G2} (Ω)[1]	Differential Output Noise Density (nV/√Hz)
0	301	142	64.2	190.67	170	5.9
6	301	63.4	84.5	95.06	95	7.8
10	301	33.2	1 k	53.54	69.3	9.3
14	301	10.2	1.15 k	17.5	57.7	10.4

[1] $R_{G2} = R_{G1} + (R_S||R_T)$.

Table 11 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

Table 12 and Table 13 list several common gain settings, associated resistor values, input impedance, and output noise density for both balanced and unbalanced input configurations.

IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

The gain from the V_{OCM} pin to $V_{O,\,dm}$ is equal to

$$2(\beta1 - \beta2)/(\beta1 + \beta2)$$

When β1 = β2, this term goes to zero and there is no differential output voltage due to the voltage on the V_{OCM} input (including noise). The extreme case occurs when one loop is open and the other has 100% feedback; in this case, the gain from V_{OCM} input to $V_{O,dm}$ is either +2 or −2, depending on which loop is closed. The feedback loops are nominally matched to within 1% in most applications, and the output noise and offsets due to the V_{OCM} input are negligible.

If the loops are intentionally mismatched by a large amount, it is necessary to include the gain term from V_{OCM} to $V_{O,\,dm}$ and account for the extra noise. For example, if β1 = 0.5 and β2 = 0.25, the gain from V_{OCM} to $V_{O,\,dm}$ is 0.67. If the V_{OCM} pin is set to 0.9 V, a differential offset voltage is present at the output of (0.9 V)(0.67) = 0.6 V. The differential output noise contribution is (5 nV/√Hz)(0.67) = 3.35 nV/√Hz. Both of these results are undesirable in most applications; therefore, it is best to use nominally matched feedback factors.

Mismatched feedback networks also result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

As a practical summarization of the previous issues, resistors of 1% tolerance produce a worst-case input CMRR of approximately 40 dB, a worst-case differential-mode output offset of 9 mV due to a 0.9 V V_{OCM} input, negligible V_{OCM} noise contribution, and no significant degradation in output balance error.

INPUT COMMON-MODE VOLTAGE RANGE

The input common-mode range at the summing nodes of the ADA4930-1/ADA4930-2 is specified as 0.3 V to 1.5 V at V_S = 3.3 V. To avoid nonlinearities, the voltage swing at the +IN and −IN terminals must be confined to these ranges.

MINIMUM R_G VALUE

Due to the wide bandwidth of the ADA4930-1/ADA4930-2, the value of R_G must be greater than or equal to 301 Ω at unity gain to provide sufficient damping in the amplifier front end. In the terminated case, R_G includes the Thevenin resistance of the source and load terminations.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4930-1/ADA4930-2 is biased at 3/10 of the total supply voltage above $-V_S$ with an internal voltage divider. The input impedance of the V_{OCM} pin is 8.4 kΩ. When relying on the internal bias, the output common-mode voltage is within about 100 mV of the expected value.

In cases where accurate control of the output common-mode level is required, it is recommended that an external source or resistor divider be used with source resistance less than 100 Ω. The output common-mode offset listed in the Specifications section assumes that the V_{OCM} input is driven by a low impedance voltage source.

It is also possible to connect the V_{OCM} input to a common-mode voltage (V_{CM}) output of an ADC. However, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ. If multiple ADA4930-1/ADA4930-2 devices share one reference output, it is recommended that a buffer be used.

CALCULATING THE INPUT IMPEDANCE FOR AN APPLICATION CIRCUIT

The effective input impedance depends on whether the signal source is single-ended or differential. For a balanced differential input signal, as shown in Figure 44, the input impedance ($R_{IN,\,dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is $R_{IN,\,dm} = 2 \times R_G$.

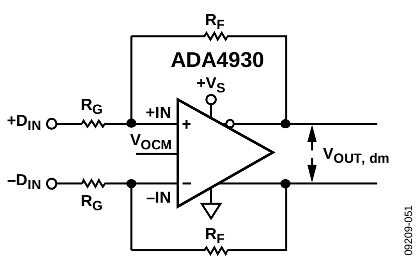


Figure 44. ADA4930-1/ADA4930-2 Configured for Balanced (Differential) Inputs

For an unbalanced single-ended input signal, as shown in Figure 45, the input impedance is

$$R_{IN,SE} = R_{G1}\ \frac{\beta 1 + \beta 2}{\beta 1(\beta 2 + 1)}$$

where:

$$\beta 1 = \frac{R_{G1}}{R_{G1} + R_{F1}}$$

$$\beta 2 = \frac{R_{G2}}{R_{G2} + R_{F2}}$$

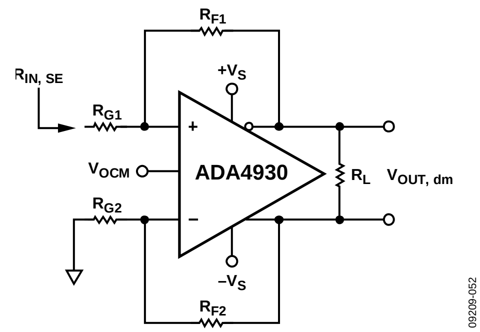


Figure 45. ADA4930-1/ADA4930-2 with Unbalanced (Single-Ended) Input

For a balanced system where $R_{G1} = R_{G2} = R_G$ and $R_{F1} = R_{F2} = R_F$, the equations simplify to

$$\beta 1 = \beta 2 = \frac{R_G}{R_G + R_F} \text{ and } R_{IN,SE} = \left(\frac{R_G}{1 - \dfrac{R_F}{2(R_G + R_F)}} \right)$$

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_{G1}. The common-mode voltage at the amplifier input terminals can be easily determined by noting that the voltage at the inverting input is equal to the noninverting output voltage divided down by the voltage divider formed by R_{F2} and R_{G2}. This voltage is present at both input terminals due to negative voltage feedback and is in phase with the input signal, thus reducing the effective voltage across R_{G1}, partially bootstrapping it.

Terminating a Single-Ended Input

This section describes the five steps that properly terminate a single-ended input to the ADA4930-1/ADA4930-2. Assume a system gain of 1, $R_{F1} = R_{F2} = 301$ Ω, an input source with an open-circuit output voltage of 2 V p-p, and a source resistance of 50 Ω. Figure 46 shows this circuit.

1. Calculate the input impedance.

   $\beta 1 = \beta 2 = 301/602 = 0.5$ and $R_{IN} = 401.333$ Ω

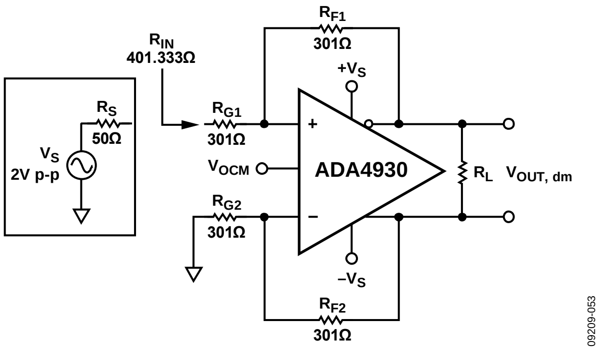


Figure 46. Single-Ended Input Impedance R_{IN}

2. Add a termination resistor, R_T. To match the 50 Ω source resistance, R_T is added. Because $R_T||401.33\ \Omega = 50\ \Omega$, $R_T = 57.116\ \Omega$.

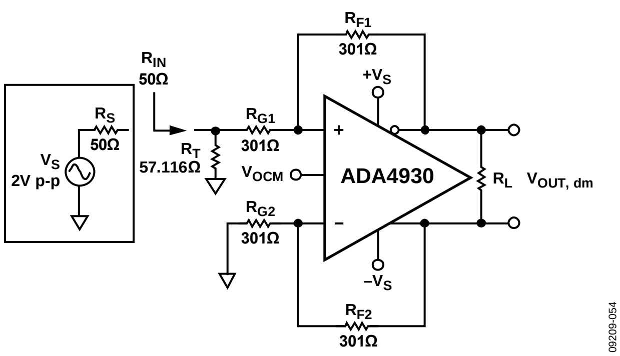


Figure 47. Adding Termination Resistor R_T

3. Replace the source-termination resistor combination with its Thevenin equivalent. The Thevenin equivalent of the source resistance R_S and the termination resistance R_T is $R_{TH} = R_S||R_T = 26.66\ \Omega$. The Thevenin equivalent of the source voltage is

$$V_{TH} = V_S \frac{R_T}{R_S + R_T} = 1.066 \text{ V p-p}$$

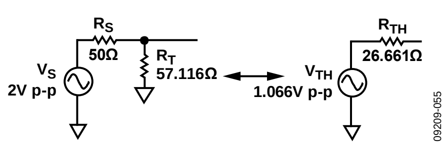


Figure 48. Thevenin Equivalent Circuit

4. Set $R_{F1} = R_{F2} = R_F$ to maintain a balanced system. Compensate the imbalance caused by R_{TH}. There are two methods available to compensate, which follow:
   - Add R_{TH} to R_{G2} to maintain balanced gain resistances and increase R_{F1} and R_{F2} to $R_F = \frac{V_S}{V_{TH}} \text{Gain}(R_G + R_{TH})$ to maintain the system gain.
   - Decrease R_{G2} to $R_{G2} = \frac{R_F \times V_{TH}}{V_S \times \text{Gain}}$ to maintain system gain and decrease R_{G1} to $(R_{G2} - R_{TH})$ to maintain balanced gain resistances.

The first compensation method is used in the Analog Devices DiffAmpCalc™ tool. Using the second compensation method, $R_{G2} = 160.498\ \Omega$ and $R_{G1} = 160.498 - 26.66 = 133.837\ \Omega$. The modified circuit is shown in Figure 49.

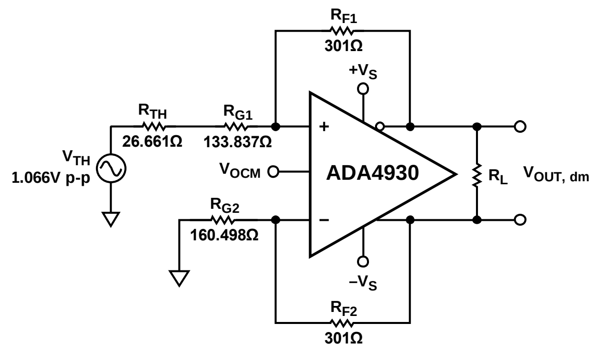


Figure 49. Thevenin Equivalent with Matched Gain Resistors

Figure 49 presents an easily manageable circuit with matched feedback loops that can be easily evaluated.

5. The modified gain resistor, R_{G1}, changes the input impedance. Repeat Step 1 through Step 4 several times using the modified value of R_{G1} from the previous iteration until the value of R_T does not change from the previous iteration. After three additional iterations, the change in R_{G1} is less than 0.1%. The final circuit is shown in Figure 50 with the closest 0.5% resistor values.

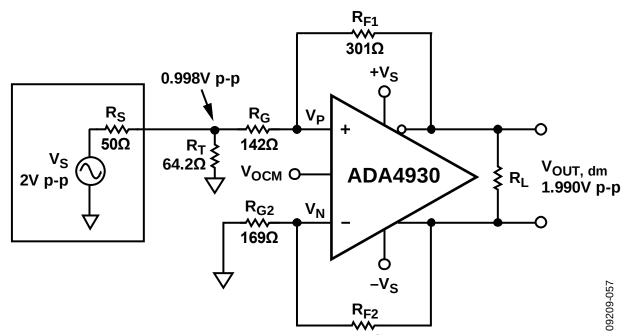


Figure 50. Terminated Single-Ended-to-Differential System with G = 1

Terminating a Single-Ended Input in a Single-Supply Applications

When the application circuit of Figure 50 is powered by a single supply, the common-mode voltage at the amplifier inputs, V_P and V_N, may have to be raised to comply with the specified input common-mode range. Two methods are available: a dc bias on the source, as shown in Figure 51, or by connecting resistors R_{CM} between each input and the supply, as shown on Figure 54.

Input Common-Mode Adjustment with DC Biased Source

To drive a 1.8 V ADC with V_{CM} = 1 V, a 3.3 V single supply minimizes the power dissipation of the ADA4930-1/ADA4930-2. The application circuit of Figure 50 on a 3.3 V single supply with a dc bias added to the source is shown in Figure 51.

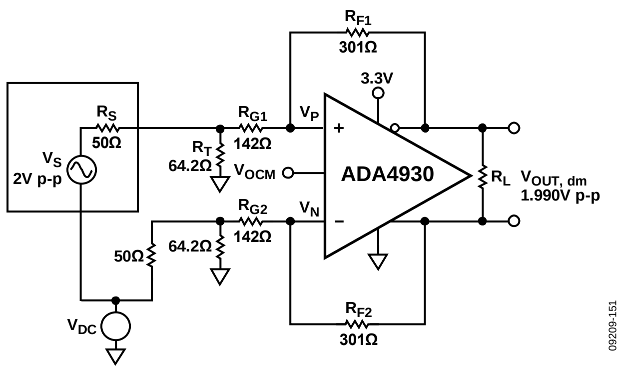


Figure 51. Single-Supply, Terminated Single-Ended-to-Differential System with G = 1

To determine the minimum required dc bias, the following steps must be taken:

1. Convert the terminated inputs to their Thevenin equivalents, as shown in the Figure 52 circuit.

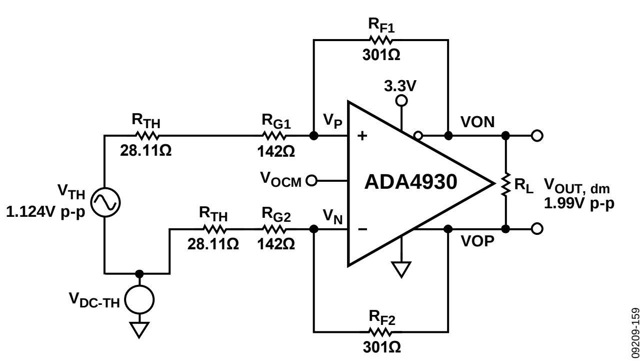


Figure 52. Thevenin Equivalent of Single-Supply Application Circuit

2. Write a nodal equation for V_P or V_N.

$$V_P = V_{TH} + V_{DC-TH} + \frac{142 + 28.11}{301 + 142 + 28.11}\left(V_{ON} - V_{TH} - V_{DC-TH}\right)$$

$$V_N = V_{DC-TH} + \frac{142 + 28.11}{301 + 142 + 28.11}\left(V_{OP} - V_{DC-TH}\right)$$

Recognize that while the ADA4930-1/ADA4930-2 is in its linear operating region, V_P and V_N are equal. Therefore, both equations in Step 2 give equal results.

3. To comply with the minimum specified input common-mode voltage of 0.3 V at V_S = 3.3 V, set the minimum value of V_P and V_N to 0.3 V.
4. Recognize that V_P and V_N are at their minimum values when V_{OP} and V_S are at their minimum (and therefore V_{ON} is at its maximum).

   Let

   $V_{P\ min} = V_{N\ min} = 0.3$ V, $V_{OCM} = V_{CM} = 1$ V, $V_{TH\ min} = -V_{TH}/2$
   $V_{ON\ max} = V_{OCM} + V_{OUT,\ dm}/4$ and $V_{OP\ min} = V_{OCM} - V_{OUT,\ dm}/4$

   Substitute conditions into the nodal equation for V_P and solve for V_{DC-TH}.

   $0.3 = -1.124/2 + V_{DC-TH} + 0.361 \times (1 + 1.99/4 + 1.124/2 - V_{DC-TH})$

   $0.3 + 0.562 - 0.361 - 0.18 - 0.203 = 0.639\ V_{DC-TH}$

   $V_{DC-TH} = 0.186$ V

   Or

   Substitute conditions into the nodal equation for V_N and solve for V_{DC-TH}.

   $0.3 = V_{DC-TH} + 0.361 \times (1 - 1.99/4 - V_{DC-TH})$

   $0.3 - 0.361 + 0.18 = 0.639 \times V_{DC-TH}$

   $V_{DC-TH} = 0.186$ V
5. Converting VDC-TH from its Thevenin equivalent results in

$$V_{DC} = \frac{R_S + R_{TH}}{R_{TH}} \times 0.186 = 0.33\ \text{V}$$

The final application circuit is shown in Figure 53. The additional dc bias of 0.33 V at the inputs ensures that the minimum input common-mode requirements are met when the source signal is bipolar with a 2 V p-p amplitude and V_{OCM} is at 1 V.

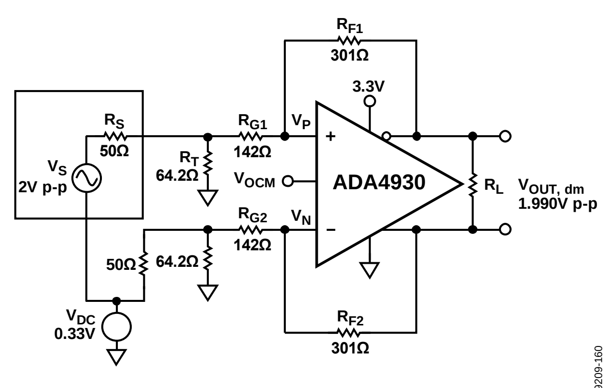


Figure 53. Single-Supply Application Circuit with DC Source Bias

Input Common-Mode Adjustment with Resistors

The circuit shown in Figure 54 shows an alternate method to bias the amplifier inputs, eliminating the dc source.

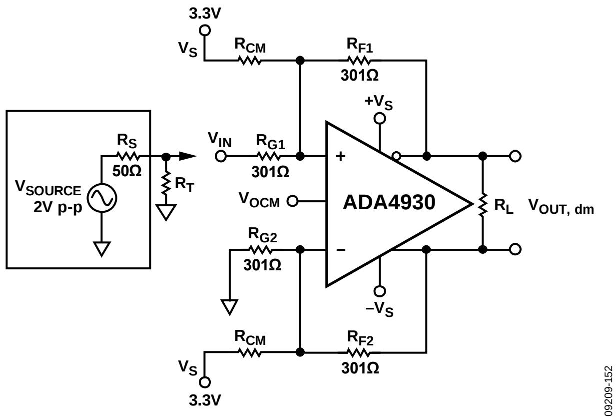


Figure 54. Single-Supply Biasing Scheme with Resistors

Define $\beta 1 = R_P/R_{F1}$ and $\beta 2 = R_N/R_{F2}$, where $R_P = R_{G1}||R_{CM}||R_{F1}$ and $R_N = R_{G2}||R_{CM}||R_{F2}$.

Set $R_{F1} = R_{F2} = R_F$ to maintain a balanced system, as shown.

Write a nodal equation at V_P and solve for V_P.

$$V_P = \frac{\beta 1\beta 2}{\beta 1+\beta 2}\left(\frac{R_F}{R_{G1}}V_{IN} + 2V_{OCM} + V_S\frac{2R_F}{R_{CM}}\right)$$

Determine VP min. This is the minimum input common-mode voltage from the Specifications section. For a 3.3 V supply, $V_{P\,min}$ = 0.3 V.

Determine the minimum input voltage, $V_{IN\,min}$ at the output of the source. Recognize that once properly terminated, the source voltage is ½ of its open circuit value. Therefore, $V_{IN\,min} = -0.5$ V.

Rearrange the V_P equation for R_{CM}

$$\frac{1}{R_{CM}} = \frac{1}{2V_S R_F}\left(\frac{\beta 1+\beta 2}{\beta 1\beta 2}V_{P\,min} - \frac{R_F}{R_{G1}}V_{IN\,min} - 2V_{OCM}\right)$$

Calculate the following:

1. $\beta 1$ and $\beta 2$. For the circuit shown in Figure 54, $\beta 1 = 0.5$ and $\beta 2 = 0.5$.
2. R_{CM} for $V_{P\,min} = 0.3$ V and $V_{IN\,min} = -0.5$ V. $R_{CM} = 9933$ Ω.
3. The new values for $\beta 1$ and $\beta 2$. $\beta 1 = 0.4925$ and $\beta 2 = 0.4925$.
4. The input impedance using the following:

$$R_{IN-SE} = R_{G1}\left(\frac{1}{1-\dfrac{V_P}{V_{INP}}}\right) = R_{G1}\left(\frac{\beta 1+\beta 2}{\beta 1+\beta 2-\dfrac{R_{F1}}{R_{G1}}\beta 1\beta 2}\right)$$

$R_{IN\text{-}SE} = 399.35$ Ω.

5. R_T, R_{TH}, and V_{TH}. $R_T = 57.16$ Ω, $R_{TH} = 26.67$ Ω, and $V_{TH} = 1.067$ V.
6. The new values for R_{G1} and R_{G2}. $R_{G2} = 160.55$ Ω and $R_{G1} = 133.88$ Ω.
7. The new values for $\beta 1$ and $\beta 2$. $\beta 1 = 0.284$ and $\beta 2 = 0.317$.
8. The new value of R_{CM}. $R_{CM} = 4759.63$ Ω.
9. Repeat Step 3 through Step 8 until the values of R_{G1} and R_{G2} remain constant between iterations. After four iterations, the final circuit is shown in Figure 55.

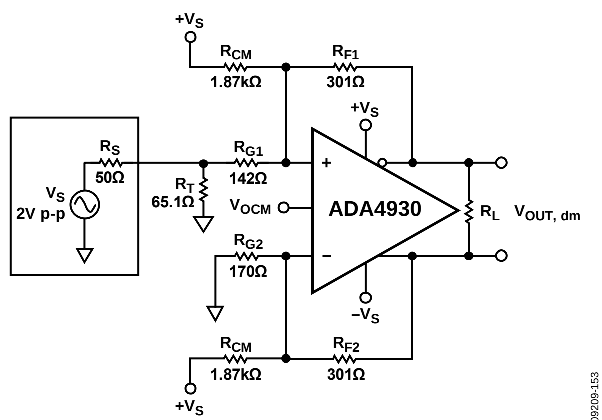


Figure 55. Single-Supply, Single-Ended Input System with Bias Resistors

LAYOUT, GROUNDING, AND BYPASSING

The ADA4930-1/ADA4930-2 are high speed devices. Realizing their superior performance requires attention to the details of high speed PCB design.

The first requirement is to use a multilayer PCB with solid ground and power planes that cover as much of the board area as possible.

Bypass each power supply pin directly to a nearby ground plane, as close to the device as possible. Use 0.1 µF high frequency ceramic chip capacitors.

Provide low frequency bulk bypassing, using 10 µF tantalum capacitors from each supply to ground.

Stray transmission line capacitance in combination with package parasitics can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation.

Signal routing should be short and direct to avoid such parasitic effects. Provide symmetrical layout for complementary signals to maximize balanced performance.

Figure 56. ADA4930-1 Ground and Power Plane Voiding in the Vicinity of R_F and R_G

Use radio frequency transmission lines to connect the driver and receiver to the amplifier.

Minimize stray capacitance at the input/output pins by clearing the underlying ground and low impedance planes near these pins (see Figure 56).

If the driver/receiver is more than one-eighth of the wavelength from the amplifier, the signal trace widths should be minimal. This nontransmission line configuration requires the underlying and adjacent ground and low impedance planes to be cleared near the signal lines.

The exposed thermal paddle is internally connected to the ground pin of the amplifier. Solder the paddle to the low impedance ground plane on the PCB to ensure the specified electrical performance and to provide thermal relief. To reduce thermal impedance further, it is recommended that the ground planes on all layers under the paddle be connected together with vias.

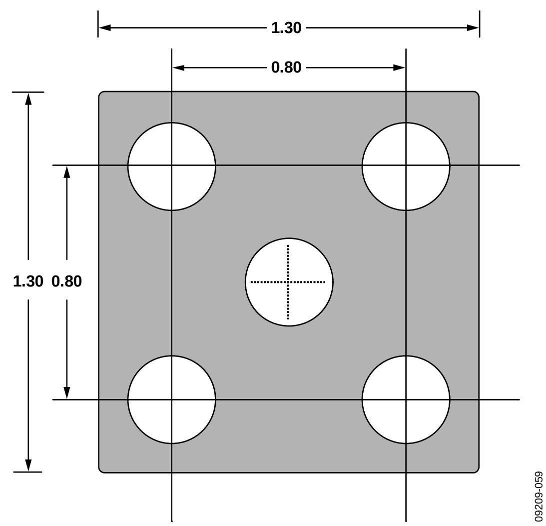


Figure 57. Recommended PCB Thermal Attach Pad Dimensions (Millimeters)

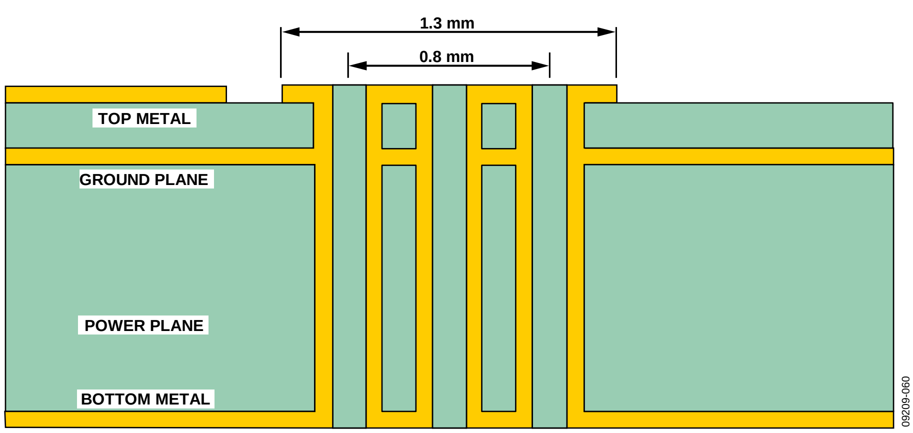


Figure 58. Cross-Section of 4-Layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in Millimeters)

HIGH PERFORMANCE ADC DRIVING

The ADA4930-1/ADA4930-2 provide excellent performance in 3.3 V single-supply applications.

The circuit shown in Figure 59 is an example of the ADA4930-1 driving an AD9255, 14-bit, 80 MSPS ADC that is specified to operate with a single 1.8 V supply. The performance of the ADC is optimized when it is driven differentially, making the best use of the signal swing available within the 1.8 V supply. The ADA4930-1 performs the single-ended-to-differential conversion, common-mode level shifting, and buffering of the driving signal.

The ADA4930-1 is configured for a single-ended input to differential output with a gain of 2 V/V. The 84.5 Ω termination resistor, in parallel with the single-ended input impedance of 95.1 Ω, provides a 50 Ω termination for the source. The additional 31.6 Ω (95 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor that drives the noninverting input.

The V_{OCM} pin is connected to the VCM output of the AD9255 and sets the output common mode of the ADA4930-1 at 0.9 V.

Note that a dc bias must be added to the signal source and its Thevenin equivalent to the gain resistor on the inverting side to ensure that the inputs of the ADA4930-1 are kept at or above the specified minimum input common-mode voltage at all times.

The 0.5 V dc bias at the signal source and the 0.314 V dc bias on the gain resistor at the inverting input set the inputs of the ADA4930-1 to ~0.48 V dc. With 1 V p-p maximum signal swing at the input, the ADA4930-1 inputs swing between 0.36 V and 0.6 V.

For a common-mode voltage of 0.9 V, each ADA4930-1 output swings between 0.401 V and 1.398 V, providing a 1.994 V p-p differential output.

A third-order, 40 MHz, low-pass filter between the ADA4930-1 and the AD9255 reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

The circuit shown in Figure 60 is an example of ½ of an ADA4930-2 driving ½ of an AD9640, a 14-bit, 80 MSPS ADC that is specified to operate with a single 1.8 V supply. The performance of the ADC is optimized when it is driven differentially, making the best use of the signal swing available within the 1.8 V supply. The ADA4930-2 performs the single-ended-to-differential conversion, common-mode level shifting, and buffering of the driving signal.

The ADA4930-2 is configured for a single-ended input to differential output with a gain of 2 V/V. The 88.5 Ω termination resistor, in parallel with the single-ended input impedance of 114.75 Ω, provides a 50 Ω termination for the source. The increased gain resistance at the inverting input balances the 50 Ω source resistance and the termination resistor that drives the noninverting input.

The V_{OCM} pin is connected to the CML output of the AD9640 and sets the output common mode of the ADA4930-2 at 1 V.

The 739 Ω resistors between each input and the 3.3 V supply provide the necessary dc bias to guarantee compliance with the input common-mode range of the ADA4930-2.

For a common-mode voltage of 1 V, each ADA4930-2 output swings between 0.501 V and 1.498 V, providing a 1.994 V p-p differential output.

A third-order, 40 MHz, low-pass filter between the ADA4930-2 and the AD9640 reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

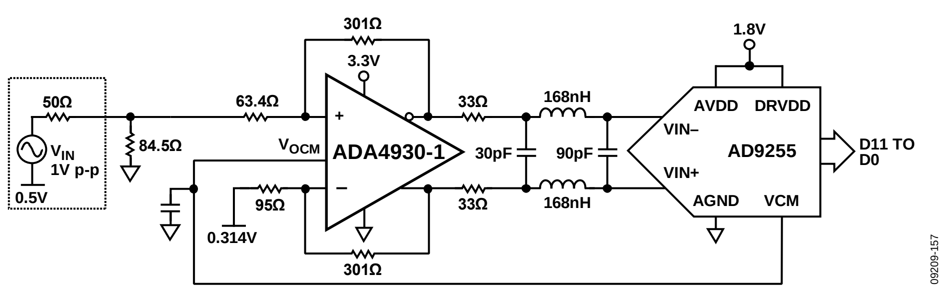


Figure 59. Driving an AD9255, 14-Bit, 80 MSPS ADC

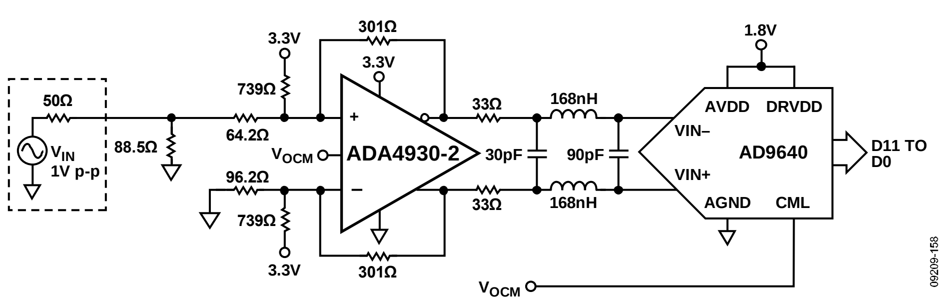
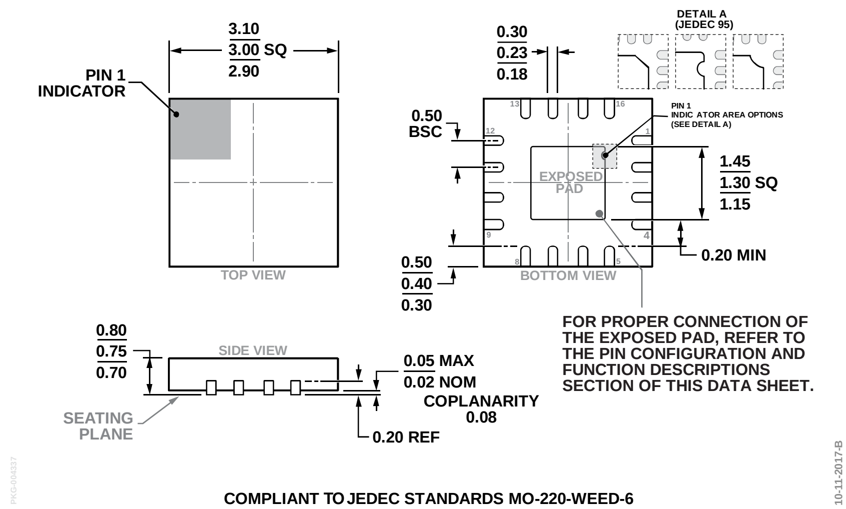


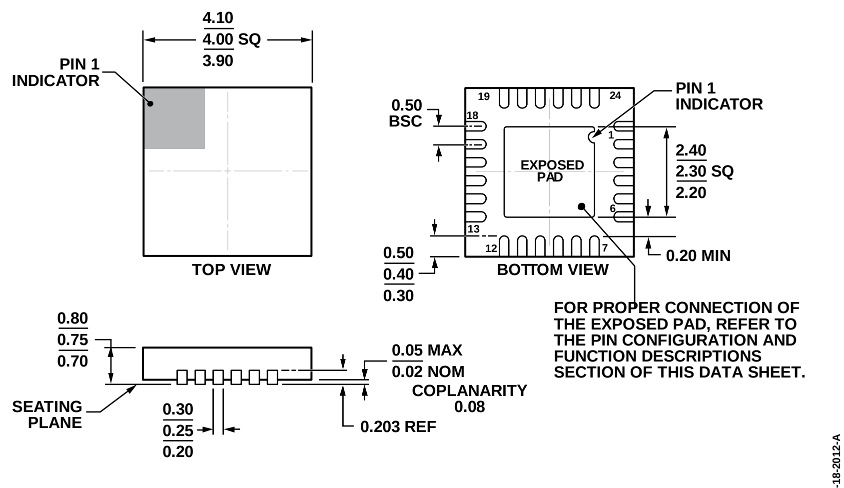
Figure 60. Driving an AD9640, 14-Bit, 80 MSPS ADC

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6

Figure 61. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-21)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 62. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
ADA4930-1YCPZ-R2	−40°C to +105°C	16-Lead LFCSP	CP-16-21	250	H1G
ADA4930-1YCPZ-RL	−40°C to +105°C	16-Lead LFCSP	CP-16-21	5,000	H1G
ADA4930-1YCPZ-R7	−40°C to +105°C	16-Lead LFCSP	CP-16-21	1,500	H1G
ADA4930-2YCPZ-R2	−40°C to +105°C	24-Lead LFCSP	CP-14-14	250	
ADA4930-2YCPZ-RL	−40°C to +105°C	24-Lead LFCSP	CP-24-14	5,000	
ADA4930-2YCPZ-R7	−40°C to +105°C	24-Lead LFCSP	CP-24-14	1,500	

[1] Z = RoHS Compliant Part.

D09209-0-11/17(D)