

MOSFET

OptiMOS™ 5 Power-Transistor, 80 V

Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target applications
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability with enlarged source interconnection

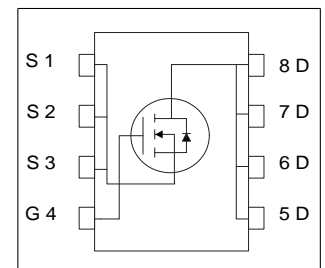


Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------------|
| V_{DS} | 80 | V |
| $R_{DS(on),max}$ | 7.5 | m Ω |
| I_D | 73 | A |
| Q_{oss} | 29 | nC |
| $Q_G(0V..10V)$ | 24 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|----------------|---------|---------------|
| BSZ075N08NS5 | PG-TSDSON-8 FL | 075N08N | - |

¹⁾ J-STD20 and JESD22

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|----------------|--------|------|----------|------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 73 47 | A | $T_C=25\text{ °C}$ $T_C=100\text{ °C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 292 | A | $T_C=25\text{ °C}$ |
| Avalanche energy, single pulse ³⁾ | E_{AS} | - | - | 104 | mJ | $I_D=20\text{ A}$, $R_{GS}=25\ \Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 69 | W | $T_C=25\text{ °C}$ |
| Operating and storage temperature | T_j, T_{stg} | -55 | - | 150 | °C | IEC climatic category; DIN IEC 68-1: 55/150/56 |

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | 1.1 | 1.8 | K/W | - |
| Device on PCB, 6 cm ² cooling area ⁴⁾ | R_{thJA} | - | - | 60 | K/W | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ See figure 3 for more detailed information

³⁾ See figure 13 for more detailed information

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------------|-------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 80 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 2.2 | 3 | 3.8 | V | $V_{DS}=V_{GS}$, $I_D=36\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 1 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 6.2 8.5 | 7.5 10.2 | m Ω | $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=5\text{ A}$ |
| Gate resistance | R_G | - | 1.3 | 2 | Ω | - |
| Transconductance | g_{fs} | 21 | 42 | - | S | $ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=20\text{ A}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance ¹⁾ | C_{iss} | - | 1600 | 2080 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance ¹⁾ | C_{oss} | - | 280 | 365 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Reverse transfer capacitance ¹⁾ | C_{rss} | - | 15 | 26 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 10 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | - | 4 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 19 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Fall time | t_f | - | 4 | - | ns | $V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=20\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |

Table 6 Gate charge characteristics²⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|------------------------------------|---------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 7.5 | - | nC | $V_{DD}=40\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge ¹⁾ | Q_{gd} | - | 5.2 | 7.8 | nC | $V_{DD}=40\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Switching charge | Q_{sw} | - | 8.1 | - | nC | $V_{DD}=40\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total ¹⁾ | Q_g | - | 24 | 29.5 | nC | $V_{DD}=40\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | $V_{plateau}$ | - | 4.6 | - | V | $V_{DD}=40\text{ V}$, $I_D=20\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | - | 20 | - | nC | $V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge ¹⁾ | Q_{oss} | - | 29 | 38.6 | nC | $V_{DD}=40\text{ V}$, $V_{GS}=0\text{ V}$ |

¹⁾ Defined by design. Not subject to production test

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---------------------------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 58 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,pulse}$ | - | - | 292 | A | $T_C=25\text{ °C}$ |
| Diode forward voltage | V_{SD} | - | 0.85 | 1.2 | V | $V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ °C}$ |
| Reverse recovery time ¹⁾ | t_{rr} | - | 37 | 74 | ns | $V_R=40\text{ V}, I_F=20\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ¹⁾ | Q_{rr} | - | 39 | 78 | nC | $V_R=40\text{ V}, I_F=20\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$ |

¹⁾ Defined by design. Not subject to production test

4 Electrical characteristics diagrams

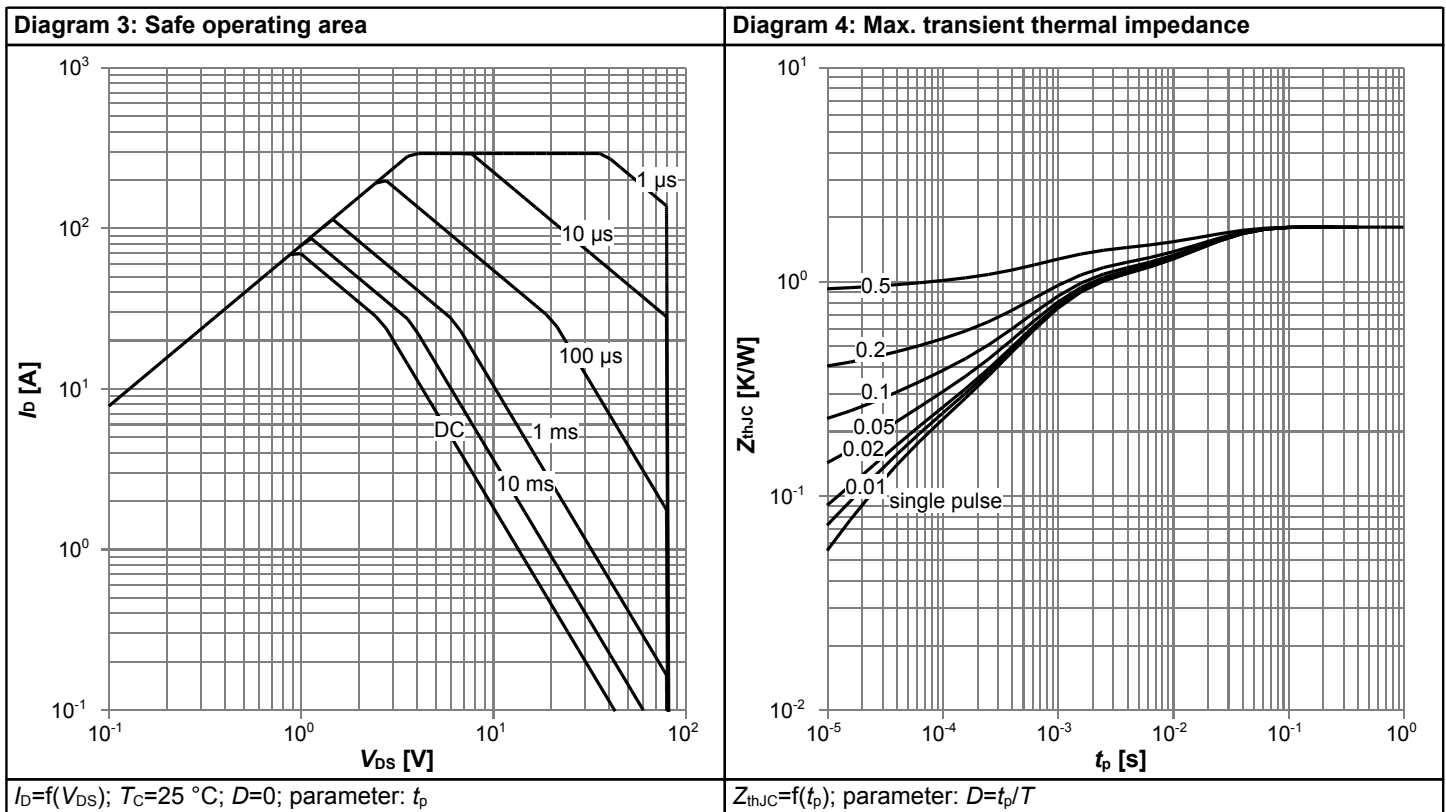
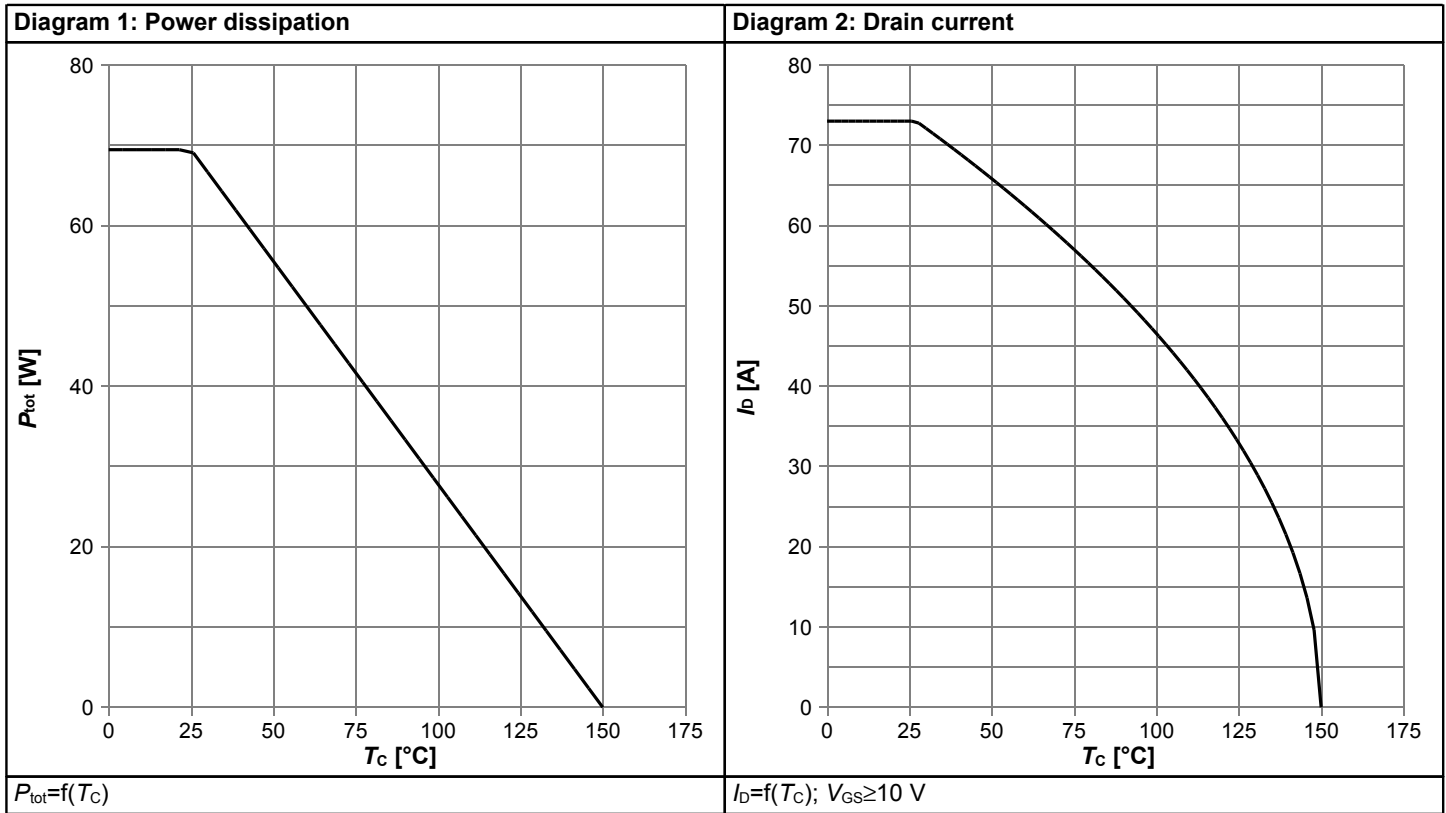
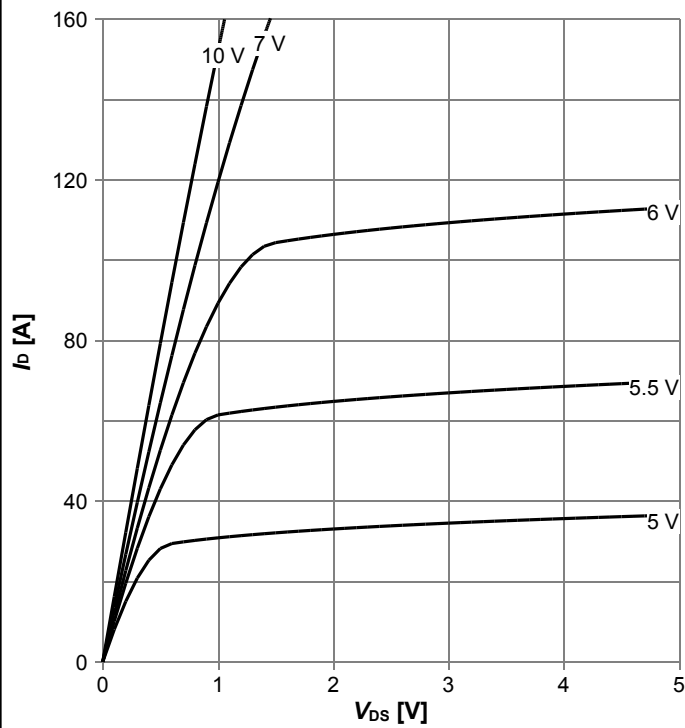
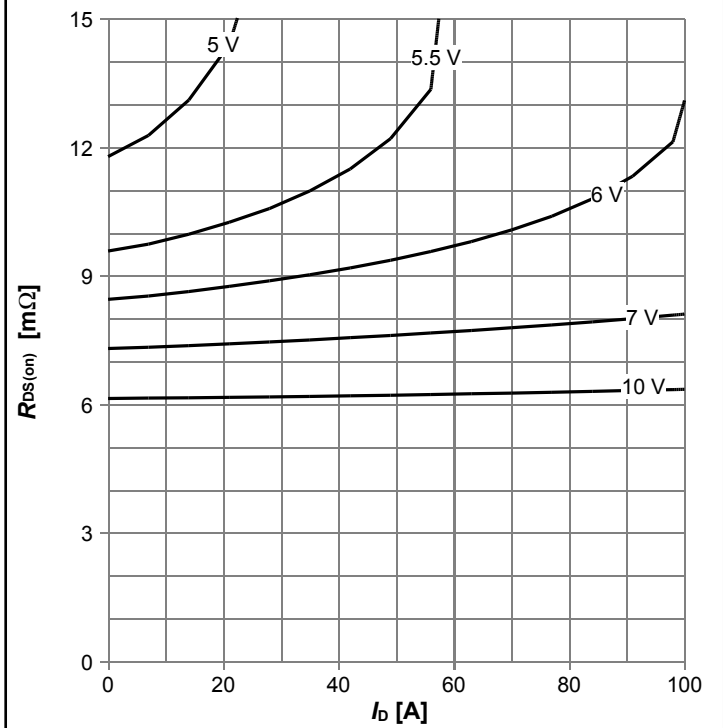


Diagram 5: Typ. output characteristics



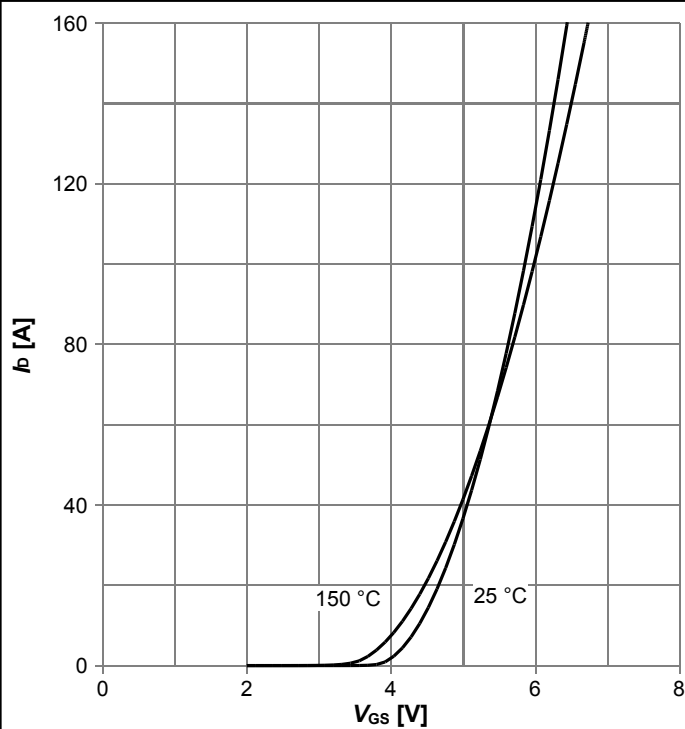
$I_D = f(V_{DS}); T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



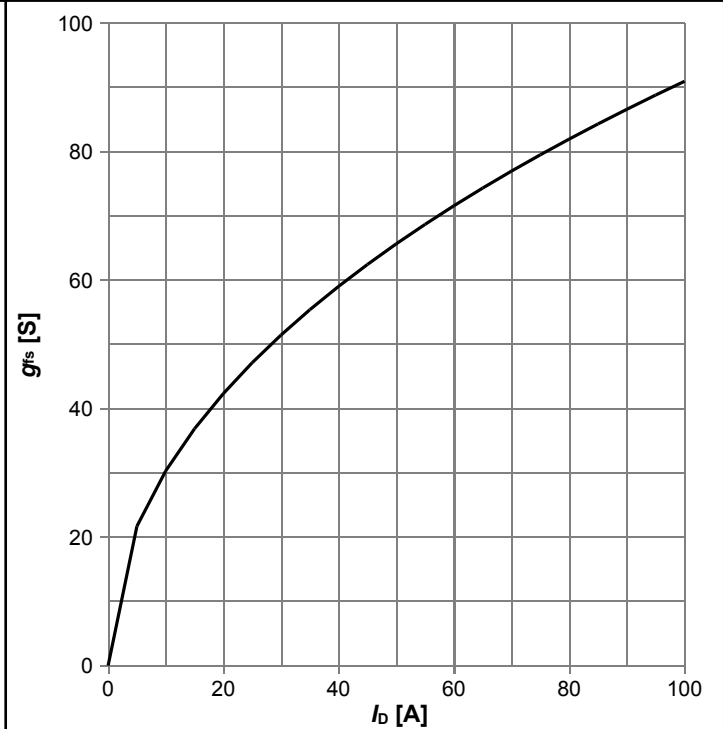
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$ parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



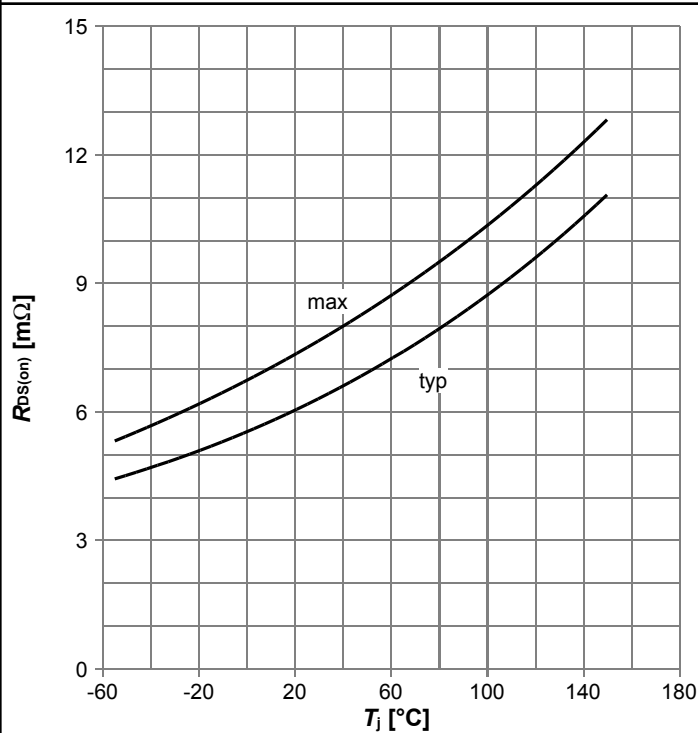
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$ parameter: T_j

Diagram 8: Typ. forward transconductance



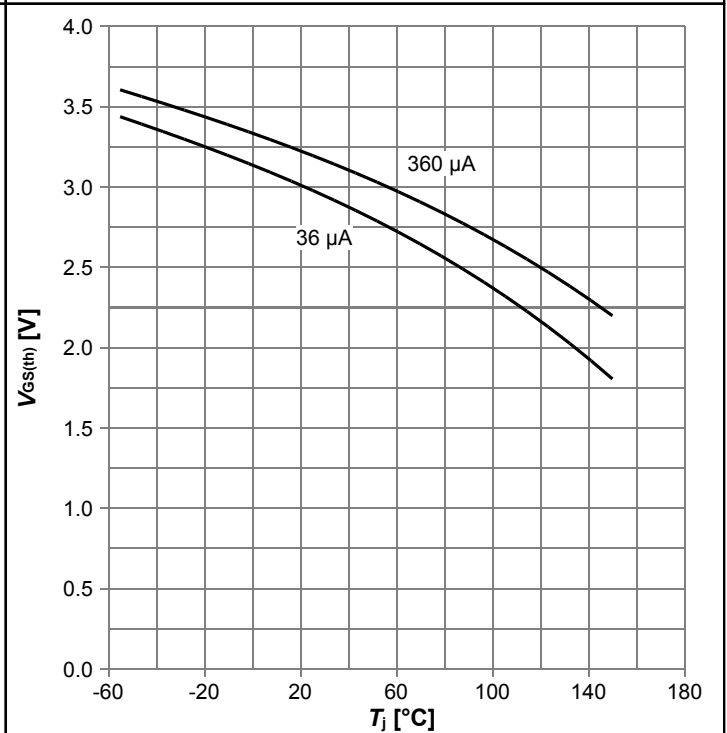
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



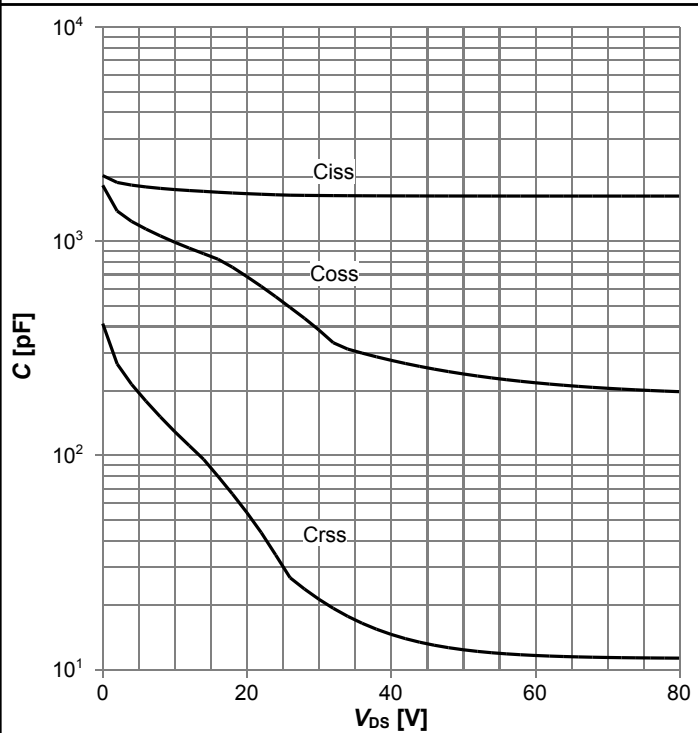
$R_{DS(on)}=f(T_j)$; $I_D=20\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



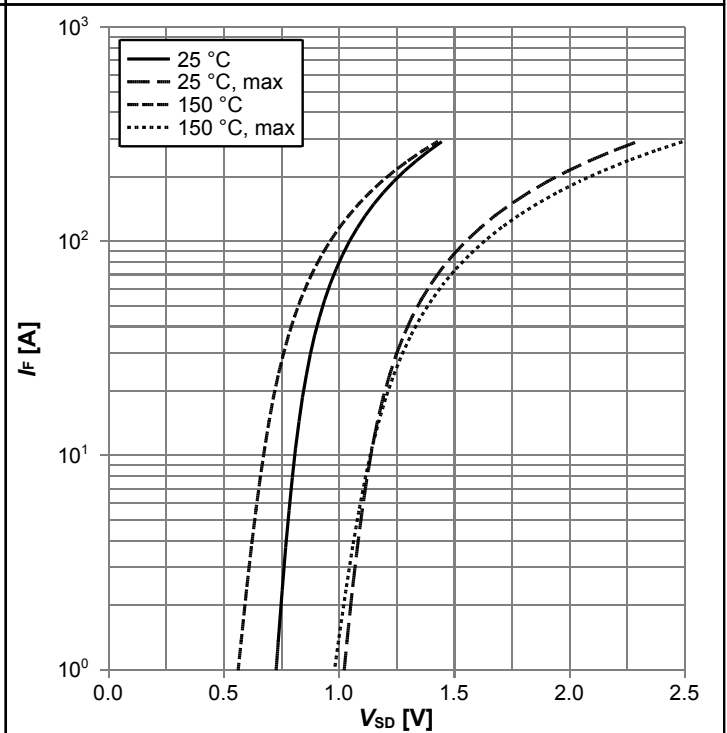
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



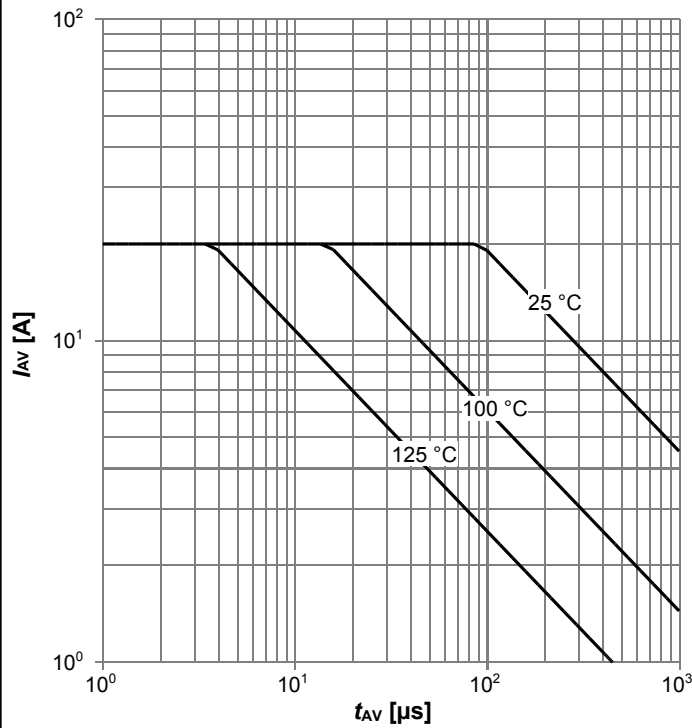
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



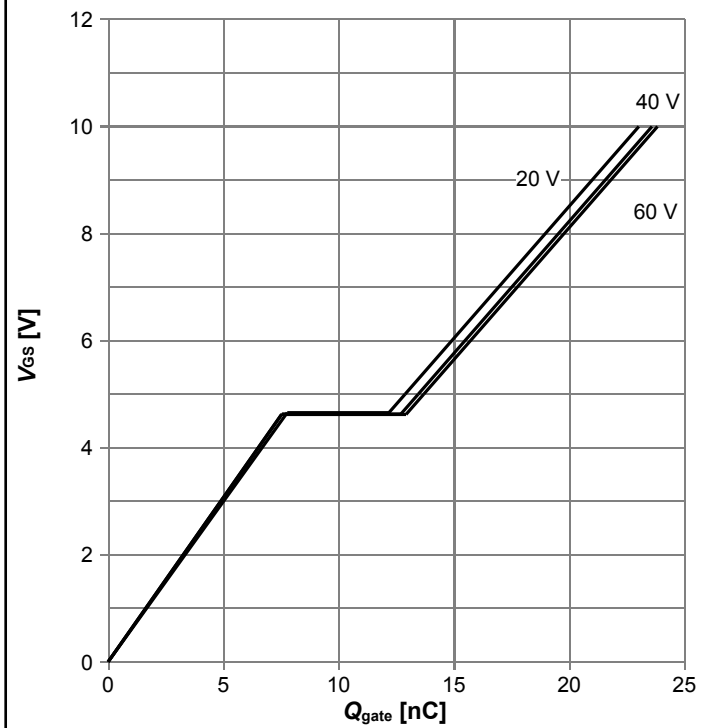
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



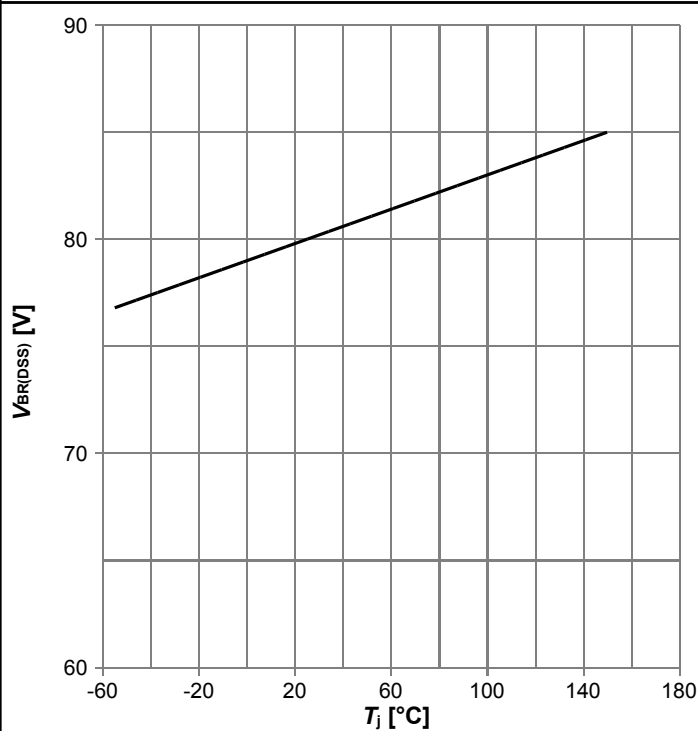
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



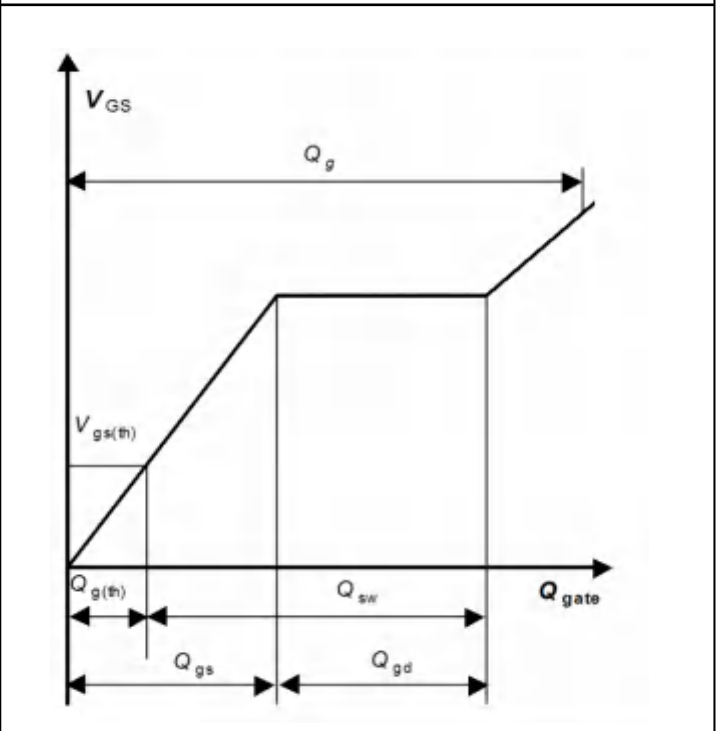
$V_{GS}=f(Q_{gate}); I_D=20 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

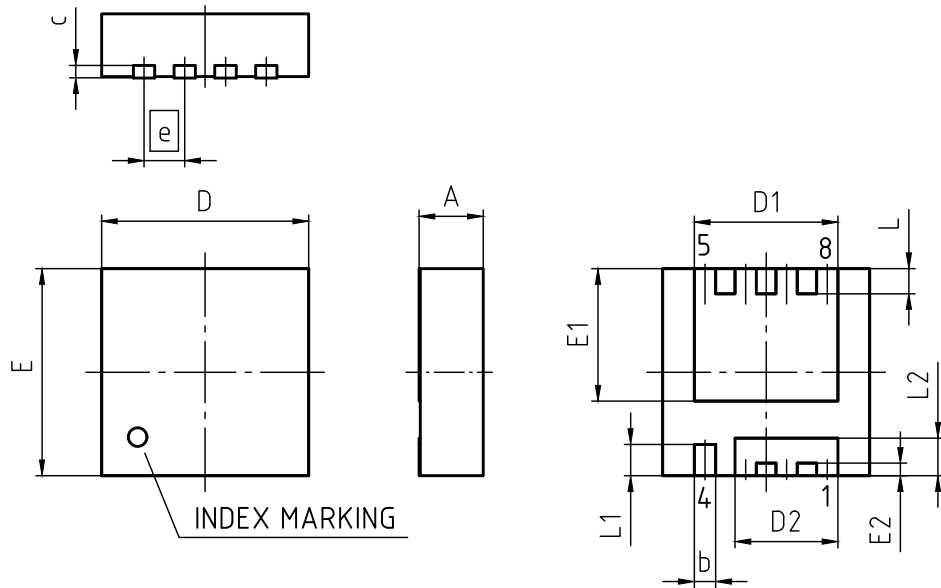


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



| PACKAGE - GROUP NUMBER: PG-TSDSON-8-U03 | | |
|--|------------------|------|
| REVISION: 03 | DATE: 20.10.2020 | |
| DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. |
| A | 0.90 | 1.10 |
| b | 0.24 | 0.44 |
| c | (0.20) | |
| D | 3.20 | 3.40 |
| D1 | 2.19 | 2.39 |
| D2 | 1.54 | 1.74 |
| E | 3.20 | 3.40 |
| E1 | 2.01 | 2.21 |
| E2 | 0.10 | 0.30 |
| e | 0.65 | |
| L | 0.30 | 0.50 |
| L1 | 0.40 | 0.60 |
| L2 | 0.50 | 0.70 |
| aaa | 0.06 | |

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

Revision History

BSZ075N08NS5

Revision: 2020-10-23, Rev. 2.3

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.1 | 2014-05-05 | Release of Final Version |
| 2.2 | 2020-08-14 | Update current rating and footnotes |
| 2.3 | 2020-10-23 | Update package drawing |

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