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MB91F585LA/B/C/D
MB91F586LA/B/C/D
MB91F587LA/B/C/D

FR81S, MB91580L Series Microcontroller Datasheet

This series has Cypress 32-bit microcontrollers for automobile motor control. They use the FR81S CPU that is compatible with the FR family.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency: 128MHz (Source oscillation= 4.0MHz, 32 multiplied (PLL clock multiplication system))
- General-purpose register: 32 bits, 16 sets
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instructions
  - Bit manipulation instructions
  - Barrel shift instructions
- High-level language support instructions
  - Function entry/exit instructions
  - Register content multi-load and store instructions
- Bit search instructions
  Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
  Overhead decrement during branch process
- Register interlock function
  Easy assembler writing
- Built-in multiplier and instruction level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
  - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and data.
  - Control access privilege in both privilege mode and user mode
- Built-in FPU (floating-point operation)
  - IEEE754 compliant
  - Floating-point register: 32 bits × 16 sets

Peripheral functions

- Clock generation (SSCG function is available)
  - Main oscillation (4 to 20 MHz)
  - PLL multiplication rate:1 to 32 times
- CR oscillation
  - Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)
  - Trimming is enabled
  - To be used as a count clock of hardware watchdog
  - MB91F585LC/F586LC/F587LC/F585LD/F586LD /F587LD: Oscillation stop feature during stand-by is not available
  - MB91F585LA/F586LA/F587LA/F585LB/F586LB/ F587LB: Oscillation stop feature during stand-by is available
- Built-in program flash memory capacity

MB91F585L: 512+64 Kbytes
MB91F586L: 768+64 Kbytes
MB91F587L: 1024+64 Kbytes

- Built-in data flash (WorkFlash) 64 Kbytes
- Built-in RAM capacity
  - Main RAM
    MB91F585L: 48 Kbytes
    MB91F586L: 64 Kbytes
    MB91F587L: 96 Kbytes
  - Backup RAM 8 Kbytes
- General-purpose ports:

MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC 98 ports
MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD 111 ports

  - Including eight I^2C pseudo open drain corresponding ports
- External bus interface
  (MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD)
  - Maximum operating frequency: 40MHz
  - 22-bit address, 16-bit data
- DMA controller
  - Up to 8 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)

- External interrupt input: 8 channels

Level ("H" / "L") or edge detection (rising or falling) enabled

- Multi-function serial communication (built-in transmission/reception FIFO memory): 5 channels

< UART (Asynchronous serial interface) >

  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer supported

<CSIO (Synchronous serial interface) >

  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detection function is provided.
  - Built-in chip selection function
  - DMA transfer supported

<LIN interface (v2.1)>

  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - LIN protocol revision2.1 supported.
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter.
  - DMA transfer supported

< I^2C >

  - Supported for 4 channels: ch.0,ch.1,ch.3, and ch4.
  - Full-duplex double buffering system, 64-byte transmission FIFO memory, 64-byte reception FIFO memory
  - Standard mode (Max. 100 kbps) / high-speed mode (Max. 400 kbps) supported
  - DMA transfer supported (for transmission only)

- CAN controller (CAN): 3 channels
  - Transfer speed: Up to 1Mbps
  - 64-transmission/reception message buffering: 3 channels
- FlexRay controller: 1unit(ch.A/ch.B)
  - FlexRay Specifications Version 2.1 supported
  - Up to 128 message buffers
  - 8K bytes of message RAM
  - Variable length of message buffers
  - Each message buffer can be allocated as a part of reception buffer, transmission buffer or reception FIFO memory
  - Host access to the message buffer via input and output buffers
  - Filtering for slot counter, cycle counter and channels
  - Maskable interrupts are supported
- PPG: 16 bits × 24 channels
- Reload timer: 16 bits × 4 channels
- A/D converter (successive approximation type)
  - 12-bit resolution: 3units(24 channels)
  - Conversion time: 1 µs
- Free-run timer: 16 bits × 6 channels (1 channel can be selected for input capture, and 1 channel for output compare.)
- Input capture: 16 bits × 8 channels (linked to the free-run timer)
- Output compare: 16 bits × 12 channels (linked to the free-run timer)
- Waveform generator: 2 units (12 channels)
- R/D converter: 1 channel (MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC)
- 10-bit D/A converter: 1 channel (MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD)
- Calibration: The hardware watchdog for CR oscillation drive

The CR oscillation frequency can be trimmed.

- Clock Supervisor
  - Anomaly supervisory feature (by damaged quartz, etc.) of external main oscillation (4MHz)
  - When anomaly is detected, clock is switched to CR.
- Up/ down counter: 2 channels

  8/16-bit Up/ down counter
- Base timer: 2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used.
  - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI

- Interrupt controller
- Interrupt request batch read
  Multiple interrupts from peripherals can be read by a series of registers.
- I/O relocation

Change of pin position of peripheral functions

- Low-power consumption mode
  - Sleep/Stop/Watch
  - Stop (Power shut-off)/Watch (Power shut-off)
- Power-on reset
- Low-voltage detection reset (external low-voltage detection)
- Low-voltage detection reset (internal low-voltage detection)
- Device package: LQFP-144
- CMOS 90 nm technology
- Power supplies
  - Single 5V power supply
  - The voltage step-down circuit brings the 5.0V down to generate 1.2V internally
  - I/O 5.0V

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1. Product Lineup

MB91580L Series Product Lineup Comparison

■ Memory size

Items	MB91F585LA MB91F585LB MB91F585LC MB91F585LD	MB91F586LA MB91F586LB MB91F586LC MB91F586LD	MB91F587LA MB91F587LB MB91F587LC MB91F587LD
Flash memory capacity (program)	512+64 Kbytes	768+64 Kbytes	1024+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	48 Kbytes	64 Kbytes	96 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

Items	MB91F585LA MB91F586LA MB91F587LA	MB91F585LB MB91F586LB MB91F587LB	MB91F585LC MB91F586LC MB91F587LC	MB91F585LD MB91F586LD MB91F587LD
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during stand-by	Provided	Provided	Not provided	Not provided
External bus interface	Not provided	Address: 22 bits Data: 16 bits	Not provided	Address: 22 bits Data: 16 bits
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	8 channels			
Output compare	12 channels			
Waveform generator	2 units (12 channels)			
16-bit reload timer	4 channels			
PPG	24 channels			
External interrupt	8 channels			
A/D converter	3 units (24 channels)			
R/D converter	Provided	Not provided	Provided	Not provided
D/A converter	Not provided	Provided	Not provided	Provided
Up/ down counter	2 channels			
Multi-function serial interface	5 channels			
CAN	64 msb × 3 channels (ch.0/ch.1/ch.2)			
FlexRay	128 msb × 1 unit (ch.A / ch.B)			
Software watchdog	Provided			
Hardware watchdog	Provided			

Items	MB91F585LA MB91F586LA MB91F587LA	MB91F585LB MB91F586LB MB91F587LB	MB91F585LC MB91F586LC MB91F587LC	MB91F585LD MB91F586LD MB91F587LD
CRC generation	1 channel			
Low-voltage detection reset (Internal low-voltage detection)	Provided			
Low-voltage detection reset (External low-voltage detection)	Provided			
Device package	LQFP-144			
Debug interface	Built-in OCD (On Chip Debug Unit)			

MB91580M Series Product Lineup Comparison

■ Memory size

Items	MB91F583MG MB91F583MH MB91F583MJ MB91F583MK	MB91F584MG MB91F584MH MB91F584MJ MB91F584MK	MB91F585MG MB91F585MH MB91F585MJ MB91F585MK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

Items	MB91F583MG MB91F584MG MB91F585MG	MB91F583MH MB91F584MH MB91F585MH	MB91F583MJ MB91F584MJ MB91F585MJ	MB91F583MK MB91F584MK MB91F585MK
System clock	On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation	Provided			
Oscillation stop feature during stand-by	Provided	Provided	Not provided	Not provided
External bus interface	Not provided			
DMA transfer	8 channels			
16-bit base timer	2 channels			
Free-run timer	6 channels			
Input capture	4 channels			
Output compare	7 channels			
Waveform generator	2 unit (7channels)			
16-bit reload timer	4 channels			
PPG	6 channels			
External interrupt	8 channels			
A/D converter	3 units (23 channels)			
R/D converter	Not provided			
D/A converter	Provided			
Up/ down counter	2 channels			
Multi-function serial interface	4 channels			
CAN	64msb × 2 channels (ch.0/ch.1)			
FlexRay	128msb × 1 unit (ch.A / ch.B)	Not provided	128msb × 1 unit (ch.A / ch.B)	Not provided
Software watchdog	Provided			
Hardware watchdog	Provided			
CRC generation	2 channels			

Items	MB91F583MG MB91F584MG MB91F585MG	MB91F583MH MB91F584MH MB91F585MH	MB91F583MJ MB91F584MJ MB91F585MJ	MB91F583MK MB91F584MK MB91F585MK
Low-voltage detection reset (Internal low-voltage detection)	Provided			
Low-voltage detection reset (External low-voltage detection)	Provided			
Device package	LQFP-100			
Debug interface	Built-in OCD (On Chip Debug Unit)			

Note:For details on the MB91580M series, see the "MB91580M/S Series HARDWARE MANUAL".

MB91580S Series Product Lineup Comparison

■ Memory size

Items	MB91F583SG MB91F583SH MB91F583SJ MB91F583SK	MB91F584SG MB91F584SH MB91F584SJ MB91F584SK	MB91F585SG MB91F585SH MB91F585SJ MB91F585SK
Flash memory capacity (program)	256+64 Kbytes	384+64 Kbytes	512+64 Kbytes
Flash memory capacity (work)	64 Kbytes		
RAM capacity (main)	32 Kbytes	48 Kbytes	48 Kbytes
RAM capacity (backup)	8 Kbytes		

■ Function

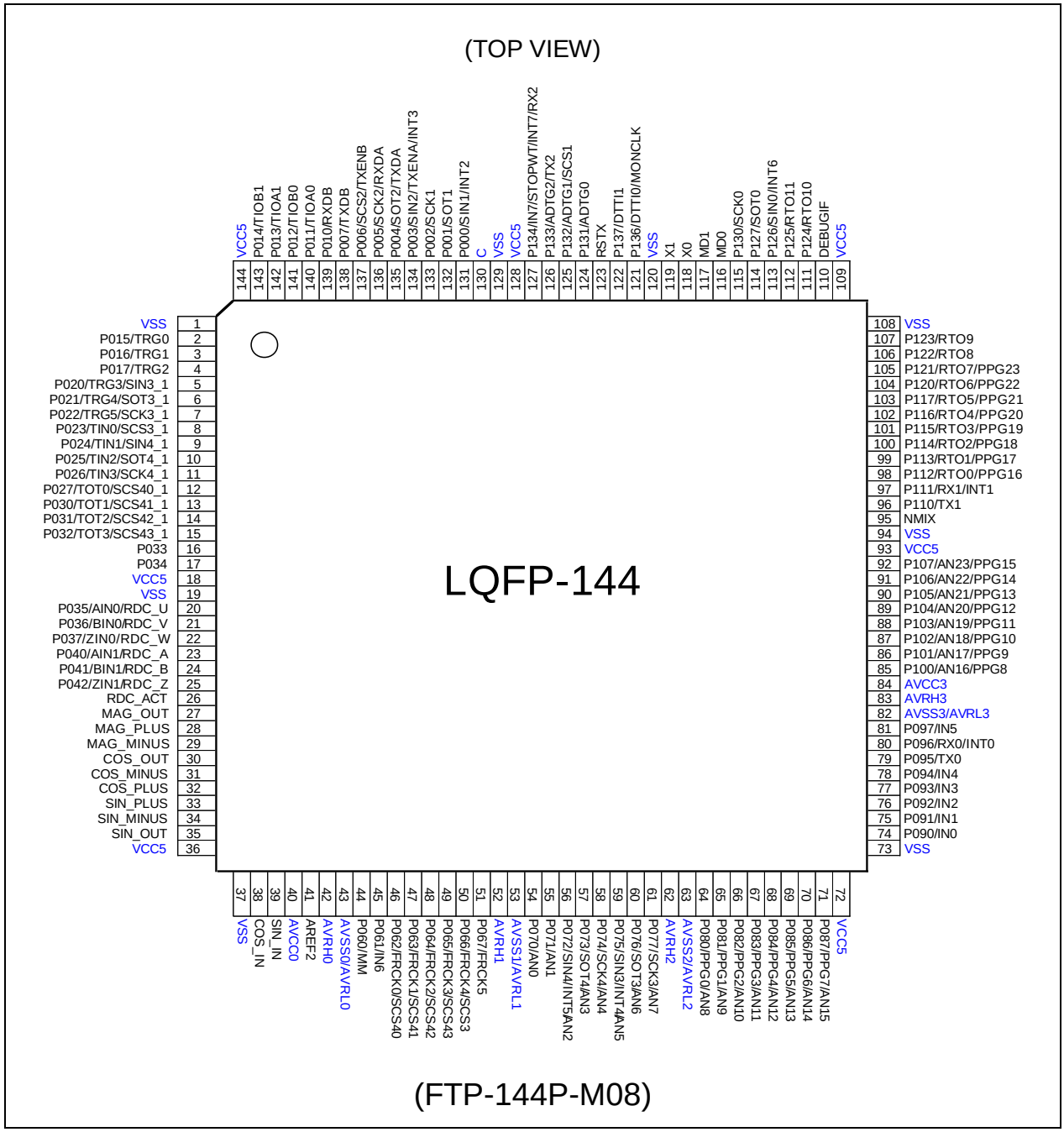
Items		MB91F583SG MB91F584SG MB91F585SG	MB91F583SH MB91F584SH MB91F585SH	MB91F583SJ MB91F584SJ MB91F585SJ	MB91F583SK MB91F584SK MB91F585SK
System clock		On-chip PLL clock multiplication system (Up to 32 times of multiplication) Minimum instruction execution time: 7.81ns (128MHz, source oscillation 4MHz × 32 times of multiplication)			
CR oscillation		Provided			
	Oscillation stop feature during stand-by	Provided	Provided	Not provided	Not provided
External bus interface		Not provided			
DMA transfer		8 channels			
16-bit base timer		2 channels			
Free-run timer		6 channels			
Input capture		4 channels			
Output compare		7 channels			
Waveform generator		2 unit (7channels)			
16-bit reload timer		4 channels			
PPG		6 channels			
External interrupt		7 channels			
A/D converter		3 units (17 channels)			
R/D converter		Not provided			
D/A converter		Provided			
Up/ down counter		2 channels			
Multi-function serial interface		2 channels			
CAN		64msb × 1 channel (ch.0)			
FlexRay		128msb × 1unit (ch.A / ch.B)	Not provided	128msb × 1unit (ch.A / ch.B)	Not provided
Software watchdog		Provided			
Hardware watchdog		Provided			
CRC generation		2 channels			

Items	MB91F583SG MB91F584SG MB91F585SG	MB91F583SH MB91F584SH MB91F585SH	MB91F583SJ MB91F584SJ MB91F585SJ	MB91F583SK MB91F584SK MB91F585SK
Low-voltage detection reset (Internal low-voltage detection)	Provided			
Low-voltage detection reset (External low-voltage detection)	Provided			
Device package	LQFP-64			
Debug interface	Built-in OCD (On Chip Debug Unit)			

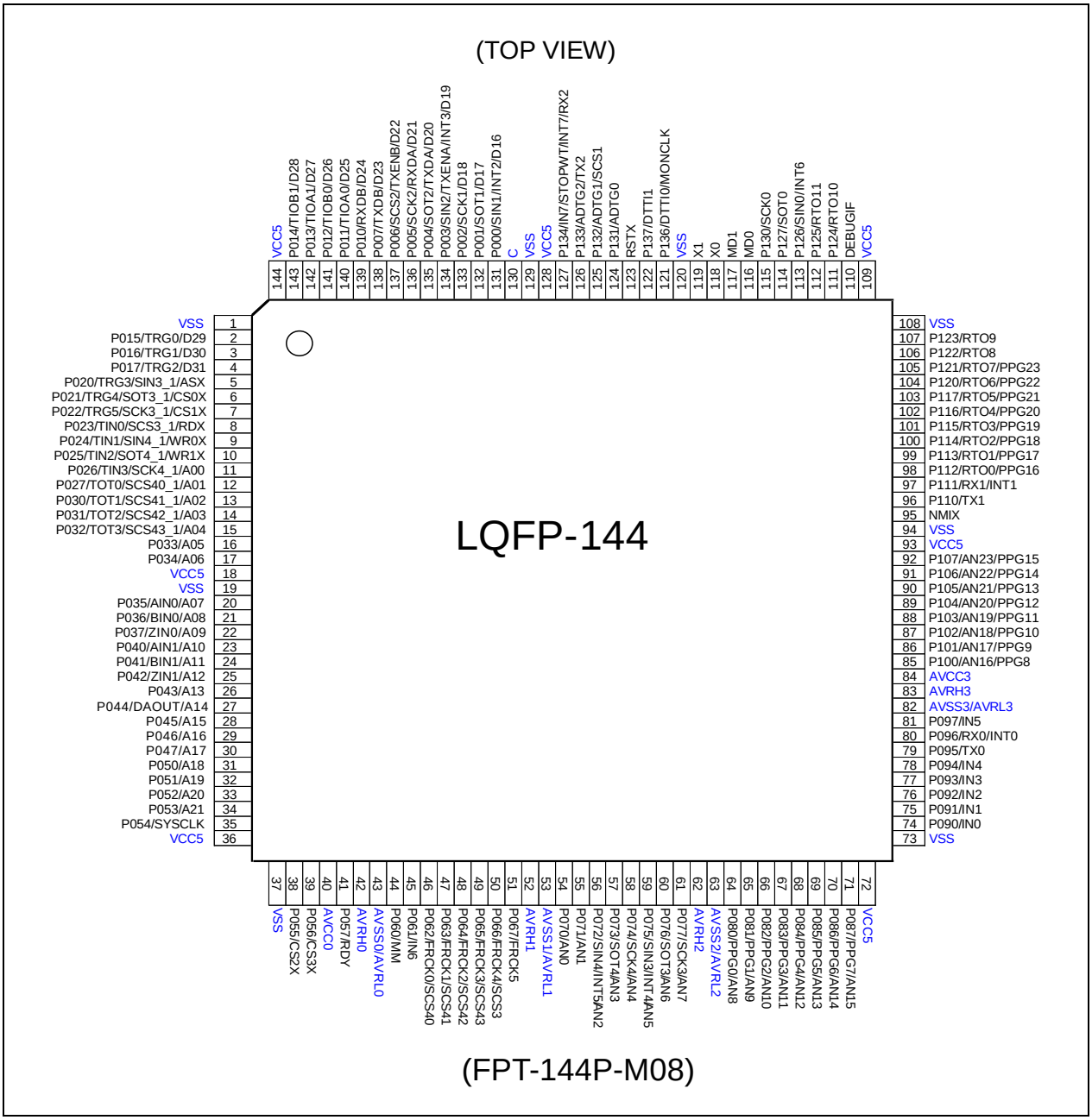
Note: For details on the MB91580S series, see the "MB91580M/S Series HARDWARE MANUAL".

2. Pin Assignment

■ LQFP-144 Pin Assignment MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



■ MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD



3. Pin Description

■ MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC

Pin No.	Pin name	I/O circuit type*	Function
118	X0	A	Main clock oscillation input pin
119	X1		Main clock oscillation output pin
95	NMIX	B	Interrupt input pin without mask
123	RSTX	B	External reset input pin
116	MD0	C	Mode pin 0 (with high-voltage control)
117	MD1	C	Mode pin 1 (with high-voltage control)
131	P000	E	General-purpose I/O port
	INT2		INT2 external interrupt input pin
	SIN1		Multi-function serial ch.1 serial data input pin
132	P001	K	General-purpose I/O port
	SOT1		Multi-function serial ch.1 serial data output pin/ I^2C ch.1 serial data I/O pin (SDA)
133	P002	K	General-purpose I/O port
	SCK1		Multi-function serial ch.1 clock I/O pin/ I^2C ch.1 clock I/O pin (SCL)
134	P003	O	General-purpose I/O port
	TXENA		FlexRay ch.A operation enable output pin
	INT3		INT3 external interrupt input pin
	SIN2		Multi-function serial ch.2 serial data input pin
135	P004	N	General-purpose I/O port
	TXDA		FlexRay ch.A data output pin
	SOT2		Multi-function serial ch.2 serial data output pin
136	P005	N	General-purpose I/O port
	RXDA		FlexRay ch.A data input pin
	SCK2		Multi-function serial ch.2 clock I/O pin
137	P006	N	General-purpose I/O port
	TXENB		FlexRay ch.B operation enable output pin
	SCS2		Multi-function serial ch2 serial chip select I/O pin
138	P007	N	General-purpose I/O port
	TXDB		FlexRay ch.B data output pin
139	P010	N	General-purpose I/O port
	RXDB		FlexRay ch.B data input pin
140	P011	D	General-purpose I/O port
	TIOA0		Base timer ch.0 TIOA I/O pin

Pin No.	Pin name	I/O circuit type*	Function
141	P012	D	General-purpose I/O port
	TIOB0		Base timer ch.0 TIOB I/O pin
142	P013	D	General-purpose I/O port
	TIOA1		Base timer ch.1 TIOA I/O pin
143	P014	D	General-purpose I/O port
	TIOB1		Base timer ch.1 TIOB I/O pin
2	P015	D	General-purpose I/O port
	TRG0		PPG ch.0 to ch.3 external trigger
3	P016	D	General-purpose I/O port
	TRG1		PPG ch.4 to ch.7 external trigger
4	P017	D	General-purpose I/O port
	TRG2		PPG ch.8 to ch.11 external trigger
5	P020	D	General-purpose I/O port
	TRG3		PPG ch.12 to ch.15 external trigger
	SIN3_1		Multi-function serial ch.3 serial data input pin (1)
6	P021	K	General-purpose I/O port
	TRG4		PPG16 to PPG19 external trigger
	SOT3_1		Multi-function serial ch.3 serial data output pin (1)/ I^2C ch.3 serial data I/O pin (1) (SDA)
7	P022	K	General-purpose I/O port
	TRG5		PPG ch.20 to ch.23 external trigger
	SCK3_1		Multi-function serial ch.3 clock I/O pin (1)/ I^2C ch.3 clock I/O pin (1) (SCL)
8	P023	D	General-purpose I/O port
	TIN0		Reload timer ch.0 event input pin
	SCS3_1		Multi-function serial ch.3 serial chip select I/O pin (1)
9	P024	D	General-purpose I/O port
	TIN1		Reload timer ch.1 event input pin
	SIN4_1		Multi-function serial ch.4 serial data input pin (1)
10	P025	K	General-purpose I/O port
	TIN2		Reload timer ch.2 event input pin
	SOT4_1		Multi-function serial ch.4 serial data output pin (1)/ I^2C ch.4 serial data I/O pin (1) (SDA)
11	P026	K	General-purpose I/O port
	TIN3		Reload timer ch.3 event input pin
	SCK4_1		Multi-function serial ch.4 clock I/O pin (1)/ I^2C ch.4 clock I/O pin (1) (SCL)

Pin No.	Pin name	I/O circuit type*	Function
12	P027	D	General-purpose I/O port
	TOT0		Reload timer ch.0 output pin
	SCS40_1		Multi-function serial ch.4 serial chip select 0 I/O pin (1)
13	P030	D	General-purpose I/O port
	TOT1		Reload timer ch.1 output pin
	SCS41_1		Multi-function serial ch.4 serial chip select 1 output pin (1)
14	P031	D	General-purpose I/O port
	TOT2		Reload timer ch.2 output pin
	SCS42_1		Multi-function serial ch.4 serial chip select 2 output pin (1)
15	P032	D	General-purpose I/O port
	TOT3		Reload timer ch.3 output pin
	SCS43_1		Multi-function serial ch.4 serial chip select 3 output pin (1)
16	P033	D	General-purpose I/O port
17	P034	D	General-purpose I/O port
20	P035	D	General-purpose I/O port
	AIN0		Up/ down counter ch.0 AIN input pin
	RDC_U		RDC phase U output pin
21	P036	D	General-purpose I/O port
	BIN0		Up/ down counter ch.0 BIN input pin
	RDC_V		RDC phase V output pin
22	P037	D	General-purpose I/O port
	ZIN0		Up/ down counter ch.0 ZIN input pin
	RDC_W		RDC phase W output pin
23	P040	D	General-purpose I/O port
	AIN1		Up/ down counter ch.1 AIN input pin
	RDC_A		RDC phase A output pin
24	P041	D	General-purpose I/O port
	BIN1		Up/ down counter ch.1 BIN input pin
	RDC_B		RDC phase B output pin
25	P042	D	General-purpose I/O port
	ZIN1		Up/ down counter ch.1 ZIN input pin
	RDC_Z		RDC phase Z output pin
26	RDC_ACT	J	RDC operation status output pin
27	MAG_OUT	I	RDC excitation signal output pin
28	MAG_PLUS	H	RDC excitation external input pin +
29	MAG_MINUS	H	RDC excitation external input pin -
30	COS_OUT	I	RDC COS output pin

Pin No.	Pin name	I/O circuit type*	Function
31	COS_MINUS	H	RDC COS input pin -
32	COS_PLUS	H	RDC COS input pin +
33	SIN_PLUS	H	RDC SIN input pin +
34	SIN_MINUS	H	RDC SIN input pin -
35	SIN_OUT	I	RDC SIN output pin
38	COS_IN	H	RDC COS coil earth leakage detection input pin
39	SIN_IN	H	RDC SIN coil earth leakage detection input pin
41	AREF2	I	RDC Aref output (AVcc0/2) pin
44	P060	D	General-purpose I/O port
	MM		Clock supervisor main clock missing output pin
45	P061	D	General-purpose I/O port
	IN6		16-bit input capture ch.6 external pulse input pin
46	P062	D	General-purpose I/O port
	FRCK0		Free-run timer ch.0 external clock input pin
	SCS40		Multi-function serial ch.4 serial chip select 0 I/O pin
47	P063	D	General-purpose I/O port
	FRCK1		Free-run timer ch.1 external clock input pin
	SCS41		Multi-function serial ch.4 serial chip select 1 output pin
48	P064	D	General-purpose I/O port
	FRCK2		Free-run timer ch.2 external clock input pin
	SCS42		Multi-function serial ch.4 serial chip select 2 output pin
49	P065	D	General-purpose I/O port
	FRCK3		Free-run timer ch.3 external clock input pin
	SCS43		Multi-function serial ch.4 serial chip select 3 output pin
50	P066	D	General-purpose I/O port
	FRCK4		Free-run timer ch.4 external clock input pin
	SCS3		Multi-function serial ch.3 serial chip select I/O pin
51	P067	D	General-purpose I/O port
	FRCK5		Free-run timer ch.5 external clock input pin
54	P070	F	General-purpose I/O port
	AN0		ADC analog 0 input pin
55	P071	F	General-purpose I/O port
	AN1		ADC analog 1 input pin
56	P072	G	General-purpose I/O port
	AN2		ADC analog 2 input pin
	SIN4		Multi-function serial ch.4 serial data input pin
	INT5		INT5 external interrupt input pin

Pin No.	Pin name	I/O circuit type*	Function
57	P073	M	General-purpose I/O port
	AN3		ADC analog 3 input pin
	SOT4		Multi-function serial ch.4 serial data output pin/ I^2C ch.4 serial data I/O pin (SDA)
58	P074	M	General-purpose I/O port
	AN4		ADC analog 4 input pin
	SCK4		Multi-function serial ch.4 clock I/O pin/ I^2C ch.4 clock I/O pin (SCL)
59	P075	G	General-purpose I/O port
	AN5		ADC analog 5 input pin
	SIN3		Multi-function serial ch.3 serial data input pin
	INT4		INT4 external interrupt input pin
60	P076	M	General-purpose I/O port
	AN6		ADC analog 6 input pin
	SOT3		Multi-function serial ch.3 serial data output pin/ I^2C ch.3 serial data I/O pin (SDA)
61	P077	M	General-purpose I/O port
	AN7		ADC analog 7 input pin
	SCK3		Multi-function serial ch.3 clock I/O pin / I^2C ch.3 clock I/O pin (SCL)
64	P080	F	General-purpose I/O port
	AN8		ADC analog 8 input pin
	PPG0		PPG ch.0 output pin
65	P081	F	General-purpose I/O port
	AN9		ADC analog 9 input pin
	PPG1		PPG ch.1 output pin
66	P082	F	General-purpose I/O port
	AN10		ADC analog 10 input pin
	PPG2		PPG ch.2 output pin
67	P083	F	General-purpose I/O port
	AN11		ADC analog 11 input pin
	PPG3		PPG ch.3 output pin
68	P084	F	General-purpose I/O port
	AN12		ADC analog 12 input pin
	PPG4		PPG ch.4 output pin
69	P085	F	General-purpose I/O port
	AN13		ADC analog 13 input pin
	PPG5		PPG ch.5 output pin

Pin No.	Pin name	I/O circuit type*	Function
70	P086	F	General-purpose I/O port
	AN14		ADC analog 14 input pin
	PPG6		PPG ch.6 output pin
71	P087	F	General-purpose I/O port
	AN15		ADC analog 15 input pin
	PPG7		PPG ch.7 output pin
74	P090	D	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
75	P091	D	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
76	P092	D	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
77	P093	D	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
78	P094	D	General-purpose I/O port
	IN4		16-bit input capture ch.4 external pulse input pin
79	P095	D	General-purpose I/O port
	TX0		CAN transmission data 0 output pin
80	P096	E	General-purpose I/O port
	RX0		CAN reception data 0 input pin
	INT0		INT0 external interrupt input pin
81	P097	D	General-purpose I/O port
	IN5		16-bit input capture ch.5 external pulse input pin
85	P100	F	General-purpose I/O port
	PPG8		PPG ch.8 output pin
	AN16		ADC analog 16 input pin
86	P101	F	General-purpose I/O port
	PPG9		PPG ch.9 output pin
	AN17		ADC analog 17 input pin
87	P102	F	General-purpose I/O port
	PPG10		PPG ch.10 output pin
	AN18		ADC analog 18 input pin
88	P103	F	General-purpose I/O port
	PPG11		PPG ch.11 output pin
	AN19		ADC analog 19 input pin

Pin No.	Pin name	I/O circuit type*	Function
89	P104	F	General-purpose I/O port
	PPG12		PPG ch.12 output pin
	AN20		ADC analog 20 input pin
90	P105	F	General-purpose I/O port
	PPG13		PPG ch.13 output pin
	AN21		ADC analog 21 input pin
91	P106	F	General-purpose I/O port
	PPG14		PPG ch.14 output pin
	AN22		ADC analog 22 input pin
92	P107	F	General-purpose I/O port
	PPG15		PPG ch.15 output pin
	AN23		ADC analog 23 input pin
96	P110	D	General-purpose I/O port
	TX1		CAN transmission data 1 output pin
97	P111	E	General-purpose I/O port
	RX1		CAN reception data 1 input pin
	INT1		INT1 external interrupt input pin
98	P112	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	PPG16		PPG ch.16 output pin
99	P113	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	PPG17		PPG ch.17 output pin
100	P114	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	PPG18		PPG ch.18 output pin
101	P115	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	PPG19		PPG ch.19 output pin
102	P116	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	PPG20		PPG ch.20 output pin
103	P117	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	PPG21		PPG ch.21 output pin

Pin No.	Pin name	I/O circuit type*	Function
104	P120	D	General-purpose I/O port
	RTO6		Waveform generator ch.6 output pin
	PPG22		PPG ch.22 output pin
105	P121	D	General-purpose I/O port
	RTO7		Waveform generator ch.7 output pin
	PPG23		PPG ch.23 output pin
106	P122	D	General-purpose I/O port
	RTO8		Waveform generator ch.8 output pin
107	P123	D	General-purpose I/O port
	RTO9		Waveform generator ch.9 output pin
111	P124	D	General-purpose I/O port
	RTO10		Waveform generator ch.10 output pin
112	P125	D	General-purpose I/O port
	RTO11		Waveform generator ch.11 output pin
113	P126	E	General-purpose I/O port
	SIN0		Multi-function serial ch.0 serial data input pin
	INT6		INT6 external interrupt input pin
114	P127	K	General-purpose I/O port
	SOT0		Multi-function serial ch.0 serial data output pin/ I^2C ch.0 serial data I/O pin (SDA)
115	P130	K	General-purpose I/O port
	SCK0		Multi-function serial ch.0 clock I/O pin/ I^2C ch.0 clock I/O pin (SCL)
124	P131	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
125	P132	D	General-purpose I/O port
	ADTG1		A/D converter ch.8 to ch.15 external trigger input pin
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
126	P133	D	General-purpose I/O port
	ADTG2		A/D converter ch.16 to ch.23 external trigger input pin
	TX2		CAN transmission data 2 output pin
127	P134	E	General-purpose I/O port
	STOPWT		FlexRay Stopwatch input pin
	RX2		CAN reception data 2 input pin
	INT7		INT7 external interrupt input pin
	IN7		16-bit input capture ch.7 external pulse input pin
110	DEBUGIF	L	DEBUG I/F pin

Pin No.	Pin name	I/O circuit type*	Function
121	P136	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	MONCLK		Clock monitor output pin
122	P137	D	General-purpose I/O port
	DTTI1		Waveform generator output stop signal input pin 1
40	AVCC0	-	R/D converter power supply
84	AVCC3	-	A/D converter analog power supply
42	AVRH0	-	R/D converter upper limit reference voltage power supply
52	AVRH1	-	A/D converter upper limit reference voltage
62	AVRH2	-	A/D converter upper limit reference voltage
83	AVRH3	-	A/D converter upper limit reference voltage
43	AVSS0	-	R/D converter GND
	AVRL0		R/D converter lower limit reference voltage
53	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
63	AVSS2	-	A/D converter GND
	AVRL2		A/D converter lower limit reference voltage
82	AVSS3	-	A/D converter GND
	AVRL3		A/D converter lower limit reference voltage
130	C	-	External capacity connection output
18, 36, 93, 72, 109, 128, 144	VCC5	-	+5.0V power supply
1, 19, 37, 73, 94, 108, 120, 129	VSS	-	GND

*: For the I/O circuit types, see "I/O circuit type".

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Pin No.	Pin name	I/O circuit type[*1]	Function
118	X0	A	Main clock oscillation input pin
119	X1		Main clock oscillation output pin
95	NMIX	B	Interrupt input pin without mask
123	RSTX	B	External reset input pin
116	MD0	C	Mode pin 0 (with high-voltage control)
117	MD1	C	Mode pin 1 (with high-voltage control)
131	P000	E	General-purpose I/O port
	D16		External bus data bit16 I/O pin
	INT2		INT2 external interrupt input pin
	SIN1		Multi-function serial ch.1 serial data input pin
132	P001	K	General-purpose I/O port
	D17		External bus data bit17 I/O pin
	SOT1		Multi-function serial ch.1 serial data output pin/ I^2C ch.1 serial data I/O pin (SDA)
133	P002	K	General-purpose I/O port
	D18		External bus data bit18 I/O pin
	SCK1		Multi-function serial ch.1 clock I/O pin / I^2C ch.1 clock I/O pin (SCL)
134	P003	O	General-purpose I/O port
	D19		External bus data bit19 I/O pin
	TXENA		FlexRay ch.A operation enable output pin
	INT3		INT3 external interrupt input pin
	SIN2		Multi-function serial ch.2 serial data input pin
135	P004	N	General-purpose I/O port
	D20		External bus data bit20 I/O pin
	TXDA		FlexRay ch.A data output pin
	SOT2		Multi-function serial ch.2 serial data output pin
136	P005	N	General-purpose I/O port
	D21		External bus data bit21 I/O pin
	RXDA		FlexRay ch.A data input pin
	SCK2		Multi-function serial ch.2 clock I/O pin

Pin No.	Pin name	I/O circuit type[*1]	Function
137	P006	N	General-purpose I/O port
	D22		External bus data bit22 I/O pin
	TXENB		FlexRay ch.B operation enable output pin
	SCS2		Multi-function serial ch.2 serial chip select I/O pin
138	P007	N	General-purpose I/O port
	D23		External bus data bit23 I/O pin
	TXDB		FlexRay ch.B data output pin
139	P010	N	General-purpose I/O port
	D24		External bus data bit24 I/O pin
	RXDB		FlexRay ch.B data input pin
140	P011	D	General-purpose I/O port
	D25		External bus data bit25 I/O pin
	TIOA0		Base timer ch.0 TIOA I/O pin
141	P012	D	General-purpose I/O port
	D26		External bus data bit26 I/O pin
	TIOB0		Base timer ch.0 TIOB I/O pin
142	P013	D	General-purpose I/O port
	D27		External bus data bit27 I/O pin
	TIOA1		Base timer ch.1 TIOA I/O pin
143	P014	D	General-purpose I/O port
	D28		External bus data bit28 I/O pin
	TIOB1		Base timer ch.1 TIOB I/O pin
2	P015	D	General-purpose I/O port
	D29		External bus data bit29 I/O pin
	TRG0		PPG ch.0 to ch.3 external trigger
3	P016	D	General-purpose I/O port
	D30		External bus data bit30 I/O pin
	TRG1		PPG ch.4 to ch.7 external trigger
4	P017	D	General-purpose I/O port
	D31		External bus data bit31 I/O pin
	TRG2		PPG ch.8 to ch.11 external trigger
5	P020	D	General-purpose I/O port
	ASX		External bus address strobe output pin
	TRG3		PPG ch.12 to ch.15 external trigger
	SIN3_1		Multi-function serial ch.3 serial data input pin (1)

Pin No.	Pin name	I/O circuit type[*1]	Function
6	P021	K	General-purpose I/O port
	CS0X		External bus chip select 0 output pin
	TRG4		PPG16 to PPG19 external trigger
	SOT3_1		Multi-function serial ch.3 serial data output pin (1)/ I^2C ch.3 serial data I/O pin (1) (SDA)
7	P022	K	General-purpose I/O port
	CS1X		External bus chip select 1 output pin
	TRG5		PPG ch.20 to ch.23 external trigger
	SCK3_1		Multi-function serial ch.3 clock I/O pin (1)/ I^2C ch.3 clock I/O pin (1) (SCL)
8	P023	D	General-purpose I/O port
	RDX		External bus read strobe output pin
	TIN0		Reload timer ch.0 event input pin
	SCS3_1		Multi-function serial ch.3 serial chip select I/O pin (1)
9	P024	D	General-purpose I/O port
	WR0X		External bus write strobe 0 output pin
	TIN1		Reload timer ch.1 event input pin
	SIN4_1		Multi-function serial ch.4 serial data input pin (1)
10	P025	K	General-purpose I/O port
	WR1X		External bus write strobe 1 output pin
	TIN2		Reload timer ch.2 event input pin
	SOT4_1		Multi-function serial ch.4 serial data output pin (1)/ I^2C ch.4 serial data I/O pin (1) (SDA)
11	P026	K	General-purpose I/O port
	A00		External bus address bit0 output pin
	TIN3		Reload timer ch.3 event input pin
	SCK4_1		Multi-function serial ch.4 clock I/O pin (1)/ I^2C ch.4 clock I/O pin (1) (SCL)
12	P027	D	General-purpose I/O port
	A01		External bus address bit1 output pin
	TOT0		Reload timer ch.0 output pin
	SCS40_1		Multi-function serial ch.4 serial chip select 0 I/O pin (1)
13	P030	D	General-purpose I/O port
	A02		External bus address bit2 output pin
	TOT1		Reload timer ch.1 output pin
	SCS41_1		Multi-function serial ch.4 serial chip select 1 output pin (1)

Pin No.	Pin name	I/O circuit type[*1]	Function
14	P031	D	General-purpose I/O port
	A03		External bus address bit3 output pin
	TOT2		Reload timer ch.2 output pin
	SCS42_1		Multi-function serial ch.4 serial chip select 2 output pin (1)
15	P032	D	General-purpose I/O port
	A04		External bus address bit4 output pin
	TOT3		Reload timer ch.3 output pin
	SCS43_1		Multi-function serial ch.4 serial chip select 3 output pin (1)
16	P033	D	General-purpose I/O port
	A05		External bus address bit5 output pin
17	P034	D	General-purpose I/O port
	A06		External bus address bit6 output pin
20	P035	D	General-purpose I/O port
	A07		External bus address bit7 output pin
	AIN0		Up/ down counter ch.0 AIN input pin
21	P036	D	General-purpose I/O port
	A08		External bus address bit8 output pin
	BIN0		Up/ down counter ch.0 BIN input pin
22	P037	D	General-purpose I/O port
	A09		External bus address bit9 output pin
	ZIN0		Up/ down counter ch.0 ZIN input pin
23	P040	D	General-purpose I/O port
	A10		External bus address bit10 output pin
	AIN1		Up/ down counter ch.1 AIN input pin
24	P041	D	General-purpose I/O port
	A11		External bus address bit11 output pin
	BIN1		Up/ down counter ch.1 BIN input pin
25	P042	D	General-purpose I/O port
	A12		External bus address bit12 output pin
	ZIN1		Up/ down counter ch.1 ZIN input pin
26	P043	D	General-purpose I/O port
	A13		External bus address bit13 output pin
27	P044	P	General-purpose I/O port
	A14		External bus address bit14 output pin
	DAOUT		DAC analog output pin
28	P045	D	General-purpose I/O port
	A15		External bus address bit15 output pin

Pin No.	Pin name	I/O circuit type*	Function
29	P046	D	General-purpose I/O port
	A16		External bus address bit16 output pin
30	P047	D	General-purpose I/O port
	A17		External bus address bit17 output pin
31	P050	D	General-purpose I/O port
	A18		External bus address bit18 output pin
32	P051	D	General-purpose I/O port
	A19		External bus address bit19 output pin
33	P052	D	General-purpose I/O port
	A20		External bus address bit20 output pin
34	P053	D	General-purpose I/O port
	A21		External bus address bit21 output pin
35	P054	D	General-purpose I/O port
	SYSCLK		External bus system clock output pin
38	P055	D	General-purpose I/O port
	CS2X		External bus chip select 2 output pin
39	P056	D	General-purpose I/O port
	CS3X		External bus chip select 3 output pin
41	P057	D	General-purpose I/O port
	RDY		External bus ready input pin
44	P060	D	General-purpose I/O port
	MM		Clock supervisor main clock missing output pin
45	P061	D	General-purpose I/O port
	IN6		16-bit input capture ch.6 external pulse input pin
46	P062	D	General-purpose I/O port
	FRCK0		Free-run timer ch.0 external clock input pin
	SCS40		Multi-function serial ch.4 serial chip select 0 I/O pin
47	P063	D	General-purpose I/O port
	FRCK1		Free-run timer ch.1 external clock input pin
	SCS41		Multi-function serial ch.4 serial chip select 1 output pin
48	P064	D	General-purpose I/O port
	FRCK2		Free-run timer ch.2 external clock input pin
	SCS42		Multi-function serial ch.4 serial chip select 2 output pin
49	P065	D	General-purpose I/O port
	FRCK3		Free-run timer ch.3 external clock input pin
	SCS43		Multi-function serial ch.4 serial chip select 3 output pin

Pin No.	Pin name	I/O circuit type[*1]	Function
50	P066	D	General-purpose I/O port
	FRCK4		Free-run timer ch.4 external clock input pin
	SCS3		Multi-function serial ch.3 serial chip select I/O pin
51	P067	D	General-purpose I/O port
	FRCK5		Free-run timer ch.5 external clock input pin
54	P070	F	General-purpose I/O port
	AN0		ADC analog 0 input pin
55	P071	F	General-purpose I/O port
	AN1		ADC analog 1 input pin
56	P072	G	General-purpose I/O port
	AN2		ADC analog 2 input pin
	SIN4		Multi-function serial ch.4 serial data input pin
	INT5		INT5 external interrupt input pin
57	P073	M	General-purpose I/O port
	AN3		ADC analog 3 input pin
	SOT4		Multi-function serial ch.4 serial data output pin I^2C ch.4 serial data I/O pin (SDA)
58	P074	M	General-purpose I/O port
	AN4		ADC analog 4 input pin
	SCK4		Multi-function serial ch.4 clock I/O / I^2C ch.4 clock I/O pin (SCL)
59	P075	G	General-purpose I/O port
	AN5		ADC analog 5 input pin
	SIN3		Multi-function serial ch.3 serial data input pin
	INT4		INT4 external interrupt input pin
60	P076	M	General-purpose I/O port
	AN6		ADC analog 6 input pin
	SOT3		Multi-function serial ch.3 serial data output pin / I^2C ch.3 serial data I/O pin (SDA)
61	P077	M	General-purpose I/O port
	AN7		ADC analog 7 input pin
	SCK3		Multi-function serial ch.3 clock I/O pin / I^2C ch.3 clock I/O pin (SCL)
64	P080	F	General-purpose I/O port
	AN8		ADC analog 8 input pin
	PPG0		PPG ch.0 output pin

Pin No.	Pin name	I/O circuit type[*1]	Function
65	P081	F	General-purpose I/O port
	AN9		ADC analog 9 input pin
	PPG1		PPG ch.1 output pin
66	P082	F	General-purpose I/O port
	AN10		ADC analog 10 input pin
	PPG2		PPG ch.2 output pin
67	P083	F	General-purpose I/O port
	AN11		ADC analog 11 input pin
	PPG3		PPG ch.3 output pin
68	P084	F	General-purpose I/O port
	AN12		ADC analog 12 input pin
	PPG4		PPG ch.4 output pin
69	P085	F	General-purpose I/O port
	AN13		ADC analog 13 input pin
	PPG5		PPG ch.5 output pin
70	P086	F	General-purpose I/O port
	AN14		ADC analog 14 input pin
	PPG6		PPG ch.6 output pin
71	P087	F	General-purpose I/O port
	AN15		ADC analog 15 input pin
	PPG7		PPG ch.7 output pin
74	P090	D	General-purpose I/O port
	IN0		16-bit input capture ch.0 external pulse input pin
75	P091	D	General-purpose I/O port
	IN1		16-bit input capture ch.1 external pulse input pin
76	P092	D	General-purpose I/O port
	IN2		16-bit input capture ch.2 external pulse input pin
77	P093	D	General-purpose I/O port
	IN3		16-bit input capture ch.3 external pulse input pin
78	P094	D	General-purpose I/O port
	IN4		16-bit input capture ch.4 external pulse input pin
79	P095	D	General-purpose I/O port
	TX0		CAN transmission data 0 output pin
80	P096	E	General-purpose I/O port
	RX0		CAN reception data 0 input pin
	INT0		INT0 external interrupt input pin

Pin No.	Pin name	I/O circuit type[*1]	Function
81	P097	D	General-purpose I/O port
	IN5		16-bit input capture ch.5 external pulse input pin
85	P100	F	General-purpose I/O port
	PPG8		PPG ch.8 output pin
	AN16		ADC analog 16 input pin
86	P101	F	General-purpose I/O port
	PPG9		PPG ch.9 output pin
	AN17		ADC analog 17 input pin
87	P102	F	General-purpose I/O port
	PPG10		PPG ch.10 output pin
	AN18		ADC analog 18 input pin
88	P103	F	General-purpose I/O port
	PPG11		PPG ch.11 output pin
	AN19		ADC analog 19 input pin
89	P104	F	General-purpose I/O port
	PPG12		PPG ch.12 output pin
	AN20		ADC analog 20 input pin
90	P105	F	General-purpose I/O port
	PPG13		PPG ch.13 output pin
	AN21		ADC analog 21 input pin
91	P106	F	General-purpose I/O port
	PPG14		PPG ch.14 output pin
	AN22		ADC analog 22 input pin
92	P107	F	General-purpose I/O port
	PPG15		PPG ch.15 output pin
	AN23		ADC analog 23 input pin
96	P110	D	General-purpose I/O port
	TX1		CAN transmission data 1 output pin
97	P111	E	General-purpose I/O port
	RX1		CAN reception data 1 input pin
	INT1		INT1 external interrupt input pin
98	P112	D	General-purpose I/O port
	RTO0		Waveform generator ch.0 output pin
	PPG16		PPG ch.16 output pin

Pin No.	Pin name	I/O circuit type[*1]	Function
99	P113	D	General-purpose I/O port
	RTO1		Waveform generator ch.1 output pin
	PPG17		PPG ch.17 output pin
100	P114	D	General-purpose I/O port
	RTO2		Waveform generator ch.2 output pin
	PPG18		PPG ch.18 output pin
101	P115	D	General-purpose I/O port
	RTO3		Waveform generator ch.3 output pin
	PPG19		PPG ch.19 output pin
102	P116	D	General-purpose I/O port
	RTO4		Waveform generator ch.4 output pin
	PPG20		PPG ch.20 output pin
103	P117	D	General-purpose I/O port
	RTO5		Waveform generator ch.5 output pin
	PPG21		PPG ch.21 output pin
104	P120	D	General-purpose I/O port
	RTO6		Waveform generator ch.6 output pin
	PPG22		PPG ch.22 output pin
105	P121	D	General-purpose I/O port
	RTO7		Waveform generator ch.7 output pin
	PPG23		PPG ch.23 output pin
106	P122	D	General-purpose I/O port
	RTO8		Waveform generator ch.8 output pin
107	P123	D	General-purpose I/O port
	RTO9		Waveform generator ch.9 output pin
111	P124	D	General-purpose I/O port
	RTO10		Waveform generator ch.10 output pin
112	P125	D	General-purpose I/O port
	RTO11		Waveform generator ch.11 output pin
113	P126	E	General-purpose I/O port
	SIN0		Multi-function serial ch.0 serial data input pin
	INT6		INT6 external interrupt input pin
114	P127	K	General-purpose I/O port
	SOT0		Multi-function serial ch.0 serial data output pin/ I^2C ch.0 serial data I/O pin (SDA)

Pin No.	Pin name	I/O circuit type[*1]	Function
115	P130	K	General-purpose I/O port
	SCK0		Multi-function serial ch.0 clock I/O pin/ I^2C ch.0 clock I/O pin (SCL)
124	P131	D	General-purpose I/O port
	ADTG0		A/D converter ch.0 to ch.7 external trigger input pin
125	P132	D	General-purpose I/O port
	ADTG1		A/D converter ch.8 to ch.15 external trigger input pin
	SCS1		Multi-function serial ch.1 serial chip select I/O pin
126	P133	D	General-purpose I/O port
	ADTG2		A/D converter ch.16 to ch.23 external trigger input pin
	TX2		CAN transmission data 2 output pin
127	P134	E	General-purpose I/O port
	STOPWT		FlexRay Stopwatch input pin
	RX2		CAN reception data 2 input pin
	INT7		INT7 external interrupt input pin
	IN7		16-bit input capture ch.7 external pulse input pin
110	DEBUGIF	L	DEBUG I/F pin
121	P136	D	General-purpose I/O port
	DTTI0		Waveform generator output stop signal input pin 0
	MONCLK		Clock monitor output pin
122	P137	D	General-purpose I/O port
	DTTI1		Waveform generator output stop signal input pin 1
40	AVCC0	-	*2
84	AVCC3	-	A/D converter analog power supply
42	AVRH0	-	*2
52	AVRH1	-	A/D converter upper limit reference voltage
62	AVRH2	-	A/D converter upper limit reference voltage
83	AVRH3	-	A/D converter upper limit reference voltage
43	AVSS0	-	*3
	AVRL0		*3
53	AVSS1	-	A/D converter GND
	AVRL1		A/D converter lower limit reference voltage
63	AVSS2	-	A/D converter GND
	AVRL2		A/D converter lower limit reference voltage
82	AVSS3	-	A/D converter GND
	AVRL3		A/D converter lower limit reference voltage
130	C	-	External capacity connection output pin

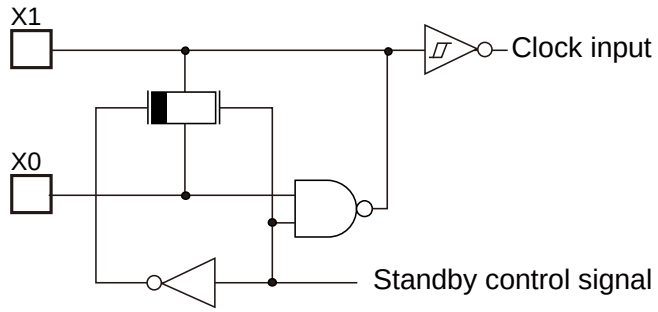
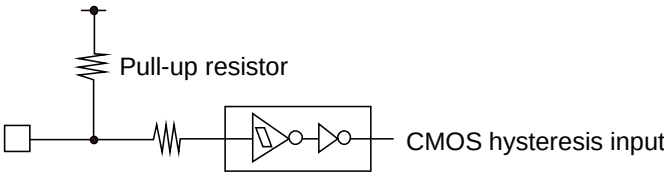
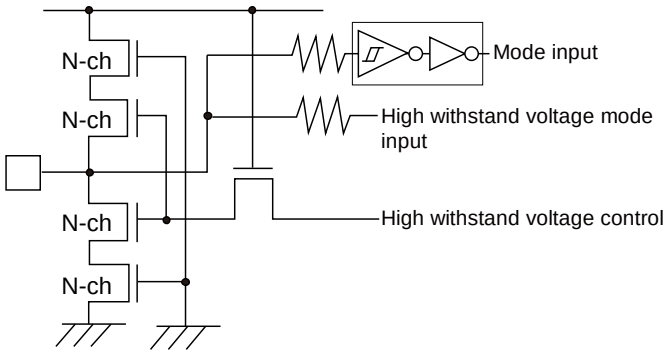
Pin No.	Pin name	I/O circuit type*	Function
18, 36, 93, 72, 109, 128, 144	VCC5	-	+5.0V power supply
1, 19, 37, 73, 94, 108, 120, 129	VSS	-	GND

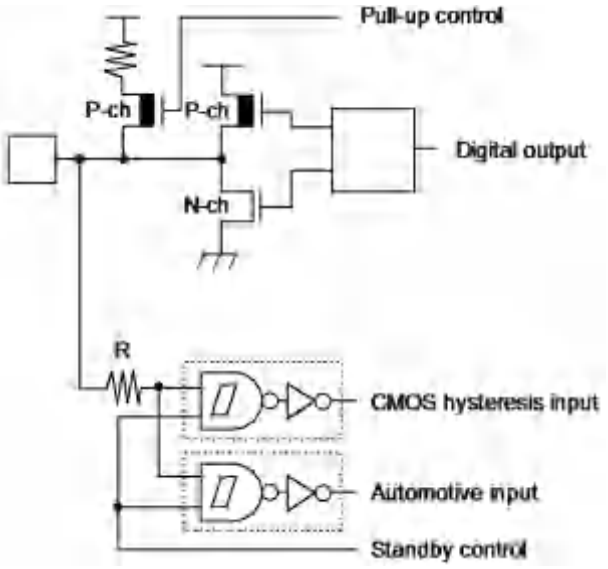
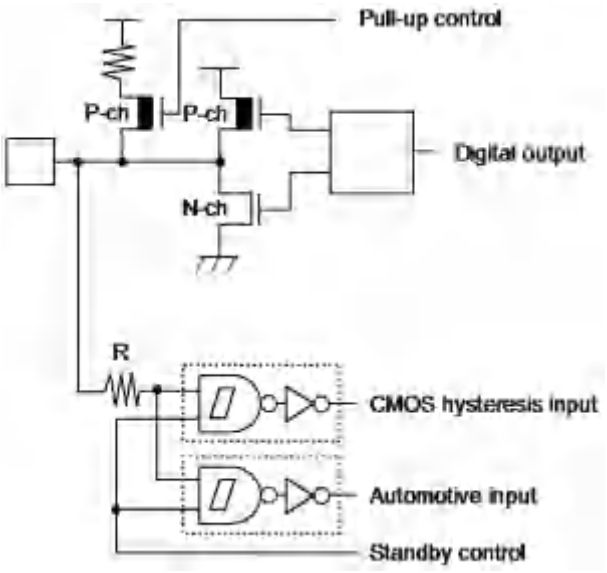
*1:For the I/O circuit types, see " I/O circuit type".

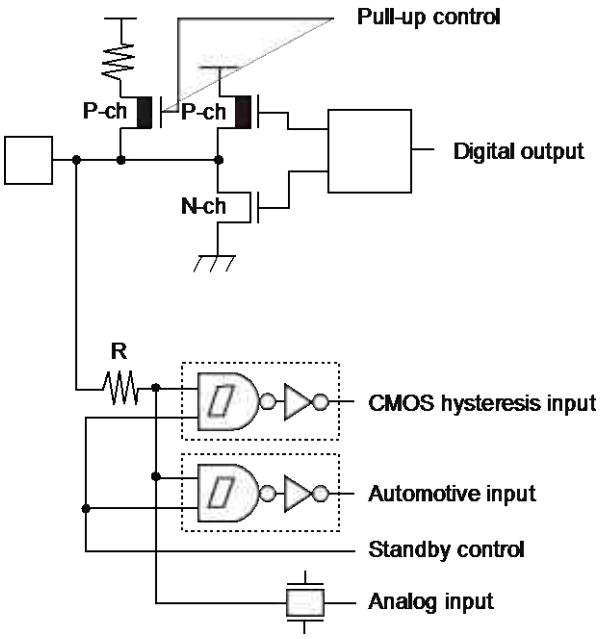
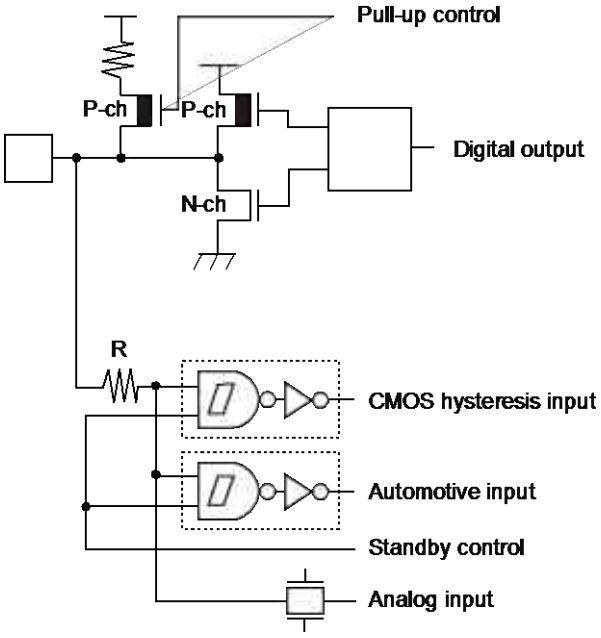
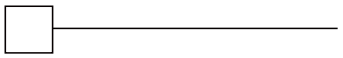
*2:The MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD do not use this pin. Connect it with the VCC5 pin.

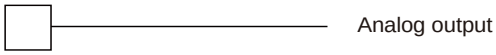
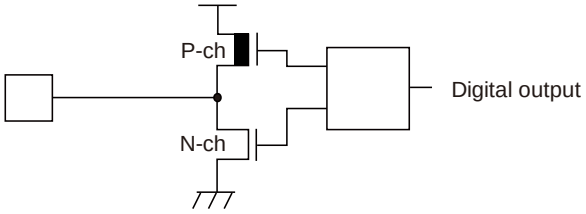
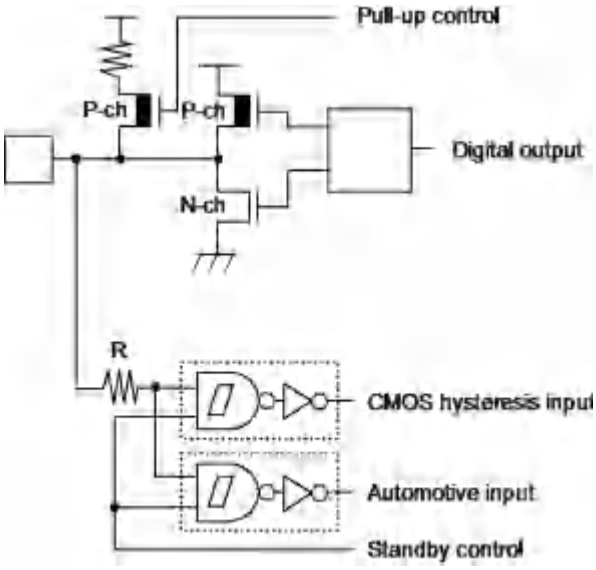
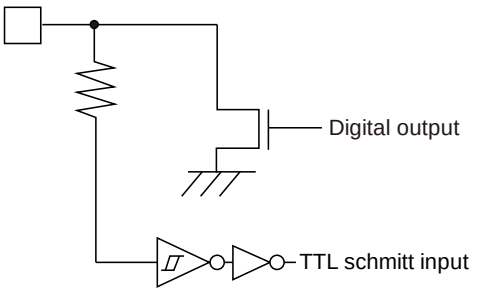
*3:The MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD do not use this pin. Connect it with the VSS pin.

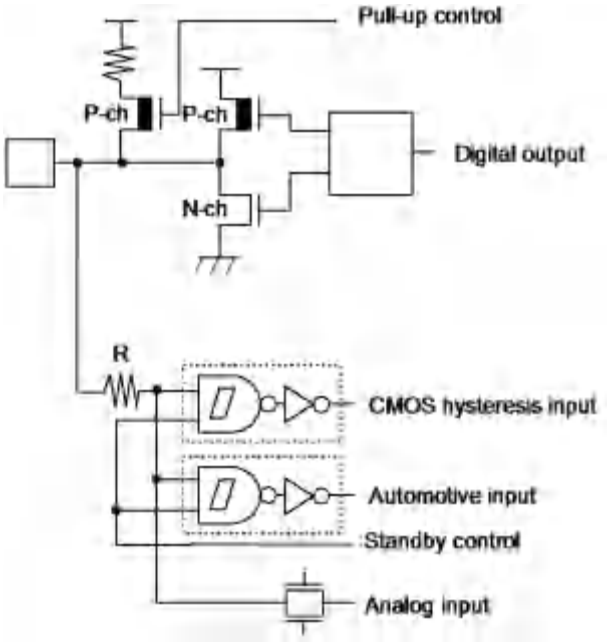
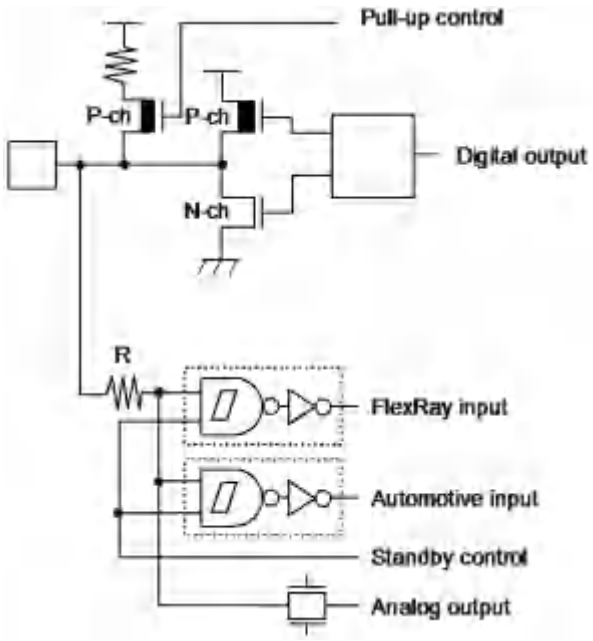
4. I/O Circuit Type

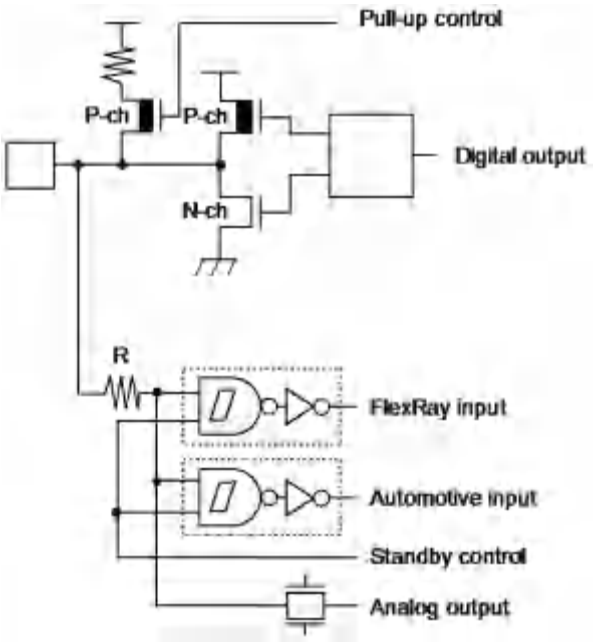
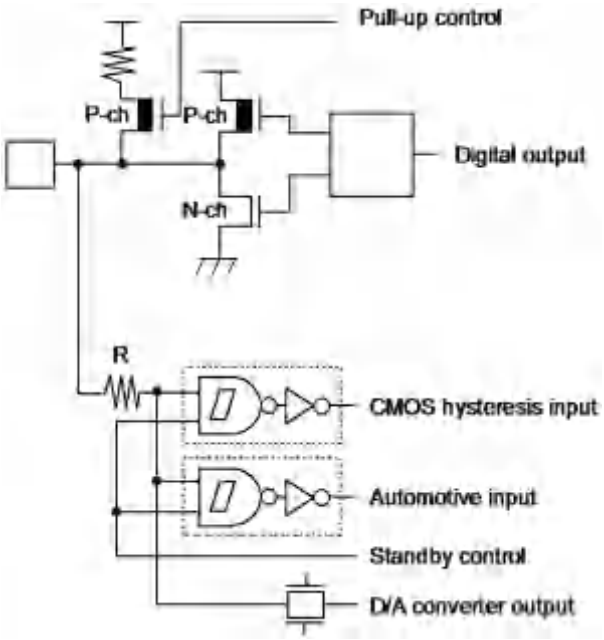
Type	Circuit	Remarks
A		Oscillation feedback resistor: Approx. 1 MΩ
B		■ CMOS hysteresis input ■ With 50 kΩ pull-up resistor
C		■ Schmitt input ■ With high withstand voltage control

Type	Circuit	Remarks
D		■ General-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
E		■ General-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.

Type	Circuit	Remarks
F		■ With analog input, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
G		■ With analog input, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.
H*		Analog input

Type	Circuit	Remarks
I*		Analog output
J*		CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA
K		■ With I^2C, general-purpose I/O port ■ CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I^2C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
L		Open drain I/O

Type	Circuit	Remarks
M		■ With analog input, I^2C, general-purpose I/O port ■ CMOS level output I_{OH}=-3mA, I_{OL}=3mA (at I^2C output) I_{OH}=-2/-5mA, I_{OL}=2/5mA (other than above) ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)
N		■ With analog output, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA ■ With 50 kΩ pull-up resistor control ■ FlexRay input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)

Type	Circuit	Remarks
O		■ With analog output, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-4mA, I_{OL}=2/4mA ■ With 50 kΩ pull-up resistor control ■ FlexRay input (0.7Vcc/0.3Vcc) During standby, the input value retains the previous value. ■ Automotive input (0.8Vcc/0.5Vcc) During standby, the input value retains the previous value.
P		■ With D/A converter output, general-purpose I/O port ■ CMOS level output I_{OH}=-2/-5mA, I_{OL}=2/5mA ■ With 50 kΩ pull-up resistor control ■ CMOS hysteresis input (0.7Vcc/0.3Vcc) ■ Automotive input (0.8Vcc/0.5Vcc)

*: MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC only

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

1. Precautions for Product Design

   This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

  Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- Recommended Operating Conditions

  Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

  Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

  No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

- Processing and Protection of Pins

  These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

  (1) Preventing Over-Voltage and Over-Current Conditions

  Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

  (2) Protection of Output Pins

  Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

  (3) Handling of Unused Input Pins

  Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

- Latch-up

  Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high-voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

  CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

  (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.

  (2) Be sure that abnormal current flows do not occur during the power-on sequence.

- Observance of Safety Regulations and Standards

  Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress. recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- Lead-Free Packaging

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- Storage of Semiconductor Devices

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C. When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Cypress Inc. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- Baking

  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

  Condition: 125°C/24 h

- Static Electricity

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

  (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

  (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

  (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
  Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

  (4) Ground all fixtures and instruments, or protect with anti-static measures.

  (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

3. Precautions for Use Environment

   Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

   For reliable performance, do the following:

   (1) Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

   (2) Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

   (3) Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.
Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

The latch-up prevention and pin processing are explained below.

■ **For latch-up prevention**

If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC and VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3) and analog input must not exceed the digital power supply (VCC5) when the power supply to the analog system is turned on or off.

In the correct power-on sequence, turn on the digital power supply voltage (VCC5) and analog power supply voltages (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3) simultaneously. Alternatively, turn on the digital power supply voltage (VCC5) first, and then turn on the analog power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3).

*: MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC only

■ **Treatment of unused pins**

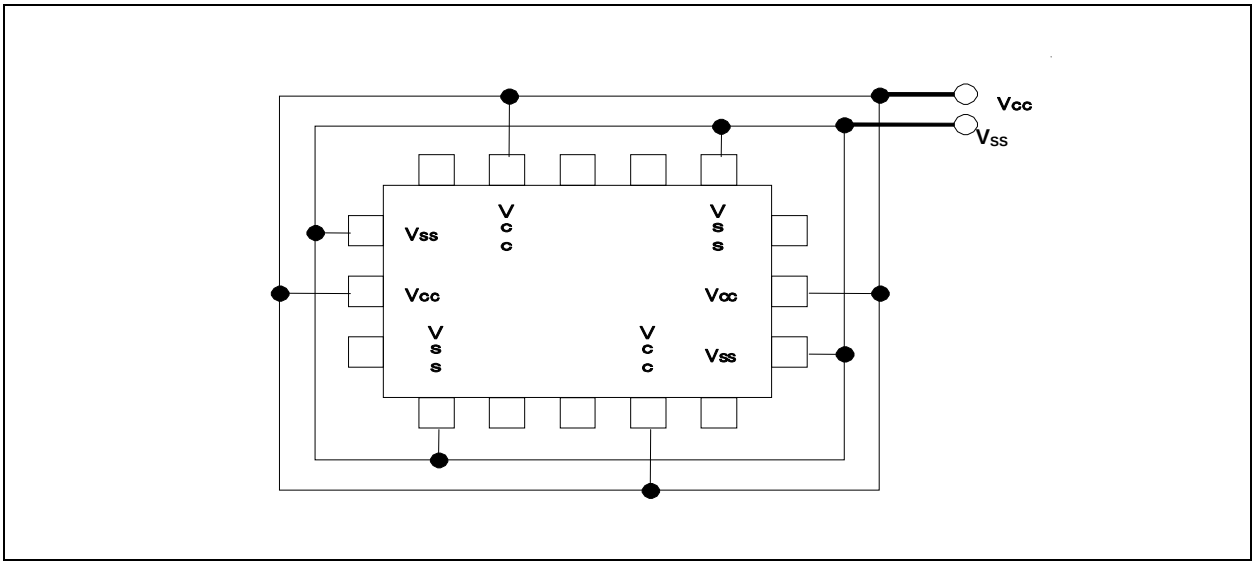
If unused input pins are left open, they may cause a permanent damage to the device due to device malfunction or latch-up. Connect a 2kΩ or higher resistor to each of unused input pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

■ **Power supply pins**

The device is designed to ensure that if the device contains multiple VCC or VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown below, all VSS power supply pins must be treated in the similar way. If multiple VCC or VSS systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Power Supply Input Pins



The power supply pins should be connected to VCC and VSS of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC and VSS pins.

■ **Crystal oscillation circuit**

An external noise to the X0 or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out X0 and X1 pins, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.
The printed circuit board artwork is recommended to surround the X0 and X1 pins by ground circuits.

■ **Mode pin (MD[1:0])**

Connect the MD[1:0] mode pin to the VCC or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and VCC or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■ **During power-on**

To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50μs or longer (between 0.2V and 2.7V) during power-on.

■ **Notes during PLL clock operation**

When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self oscillator circuit built in the PLL. This operation is not guaranteed.

■ **Treatment of R/D converter* and A/D converter power supply pins**

Connect the pins to have AVCC0 = AVCC3 = AVRH0 = AVRH1=AVRH2=AVRH3=VCC and AVSS0/AVRL0=AVSS1/AVRL1=AVSS2/AVRL2=AVSS3/AVRL3=VSS even if the R/D converter* and the A/D converter are not used.

■ **Note on using external clock**

The external clock is unsupported.
External direct clock input cannot use.

■ **Power-on sequence of R/D converter* and A/D converter power supply analog inputs**

Be sure to turn on the digital power supply (VCC5) first, and then turn on the R/D converter* and A/D converter power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3, AVRL0*, AVRL1, AVRL2, AVRL3) and analog inputs (MAG_PLUS*, MAG_MINUS*, COS_PLUS*, COS_MINUS*, SIN_PLUS*, SIN_MINUS*, COS_IN*, SIN_IN*, AN0 to AN23). Also, turn off the R/D converter* and A/D converter power supplies (AVCC0*, AVCC3, AVRH0*, AVRH1, AVRH2, AVRH3, AVRL0*, AVRL1, AVRL2, AVRL3) and analog inputs (MAG_PLUS*, MAG_MINUS*, COS_PLUS*, COS_MINUS*, SIN_PLUS*, SIN_MINUS*, COS_IN*, SIN_IN*, AN0 to AN23) first, and then turn off the digital power supply (VCC5). When the AVRH0*, AVRH1, AVRH2, and AVRH3 pin voltages are turned on or off, they must not exceed AVCC0* and AVCC3. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVCC0* or AVCC3. (However, the analog power supply voltage and digital power supply voltage can be turned on or off simultaneously.)

■ **Treatment of C pin**

This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

*: MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC only

7. Application Notes

■ **Function Switching of a Multiplexed Port**

To switch between the port function and the multiplexed pin function, use the PFR (port function register). However, if a pin is also used for an external bus, its function is switched by the external bus setting. For details, see "I/O PORTS" in Hardware Manual.

*: MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD only

■ **Low-power Consumption Mode**

To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in the "Activating the sleep mode, watch mode, or stop mode" or the "Activating the watch mode (power-off) or stop mode(power-off)" of "POWER CONSUMPTION CONTROL" in Hardware Manual.

Take the following notes when using a monitor debugger.

Do not set a break point for the low-power consumption transition program.

Do not execute an operation step for the low-power consumption transition program.

■ **Notes When Writing Data in a Register Having the Status Flag**

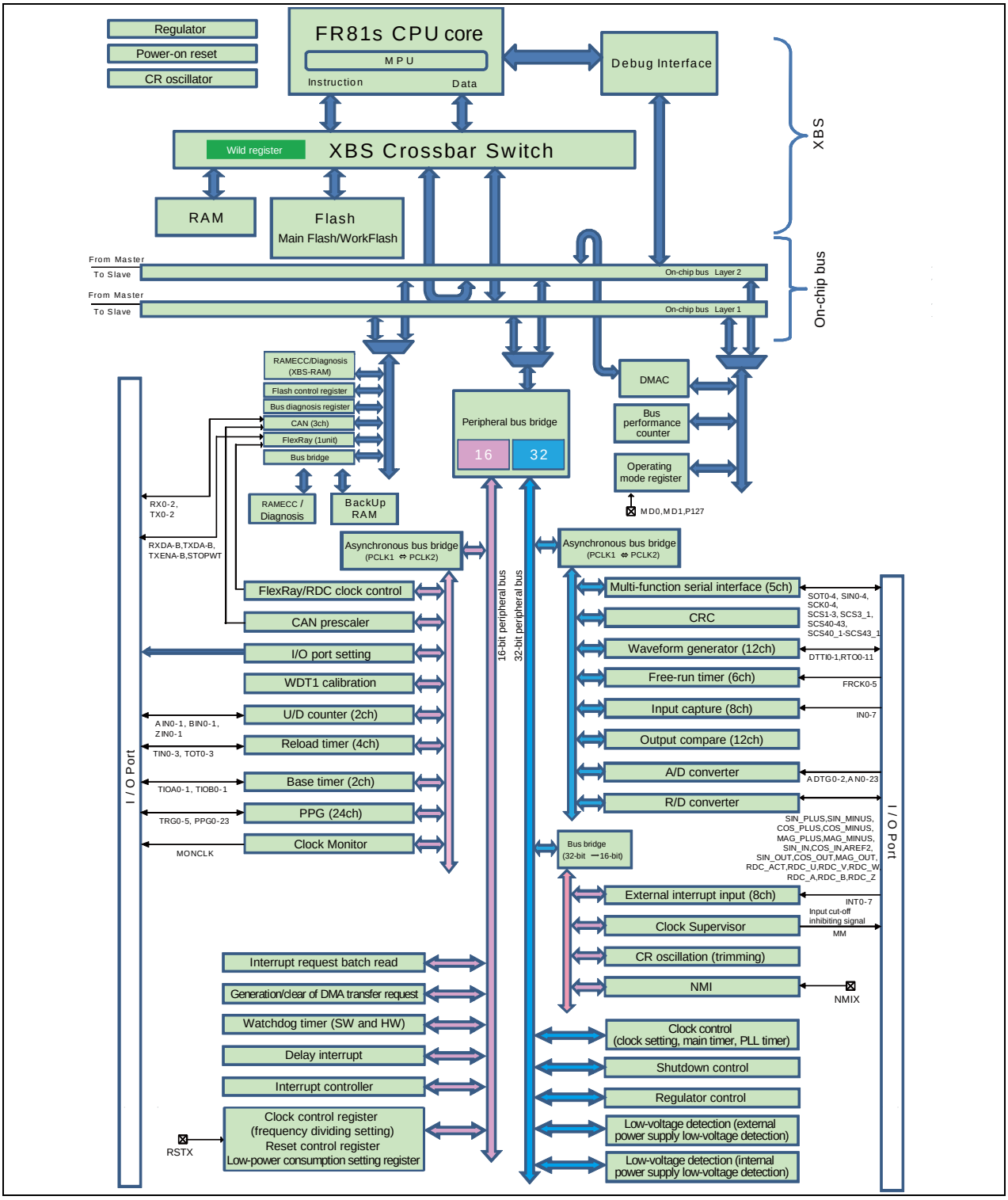
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, take care not to clear its status flag erroneously.

The program must be written not to clear the flag to the status bit, and to set the control bits to have the desired value. Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) The Byte, Half-word, or Word access must be used to write data in the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

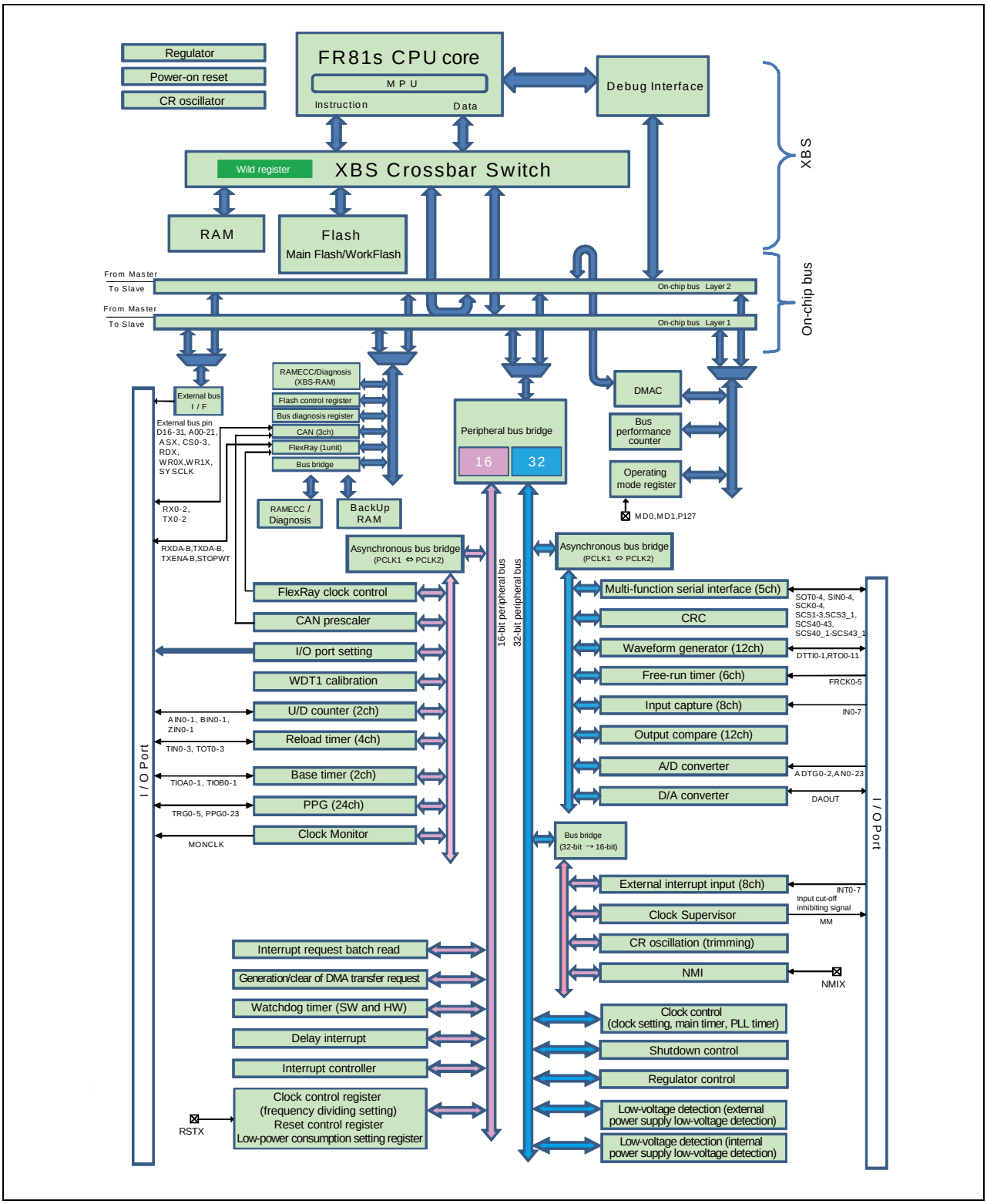
Note:These points can be ignored because the bit instructions already take the points into consideration for registers that support read-modify-write (RMW) operations. These points must be considered when using the bit instructions for registers that do not support RMW operations.

8. Block Diagram

MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC

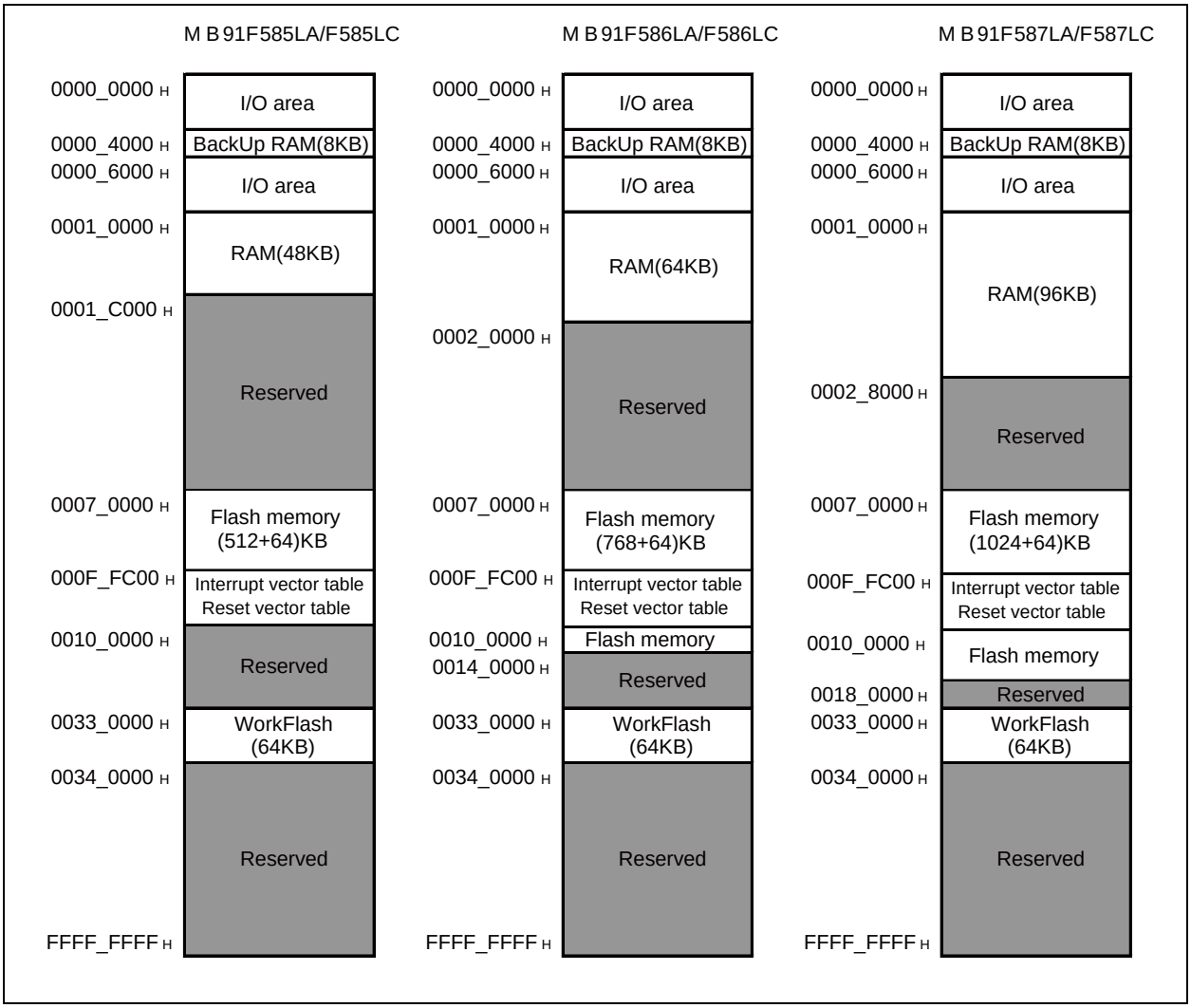


MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD

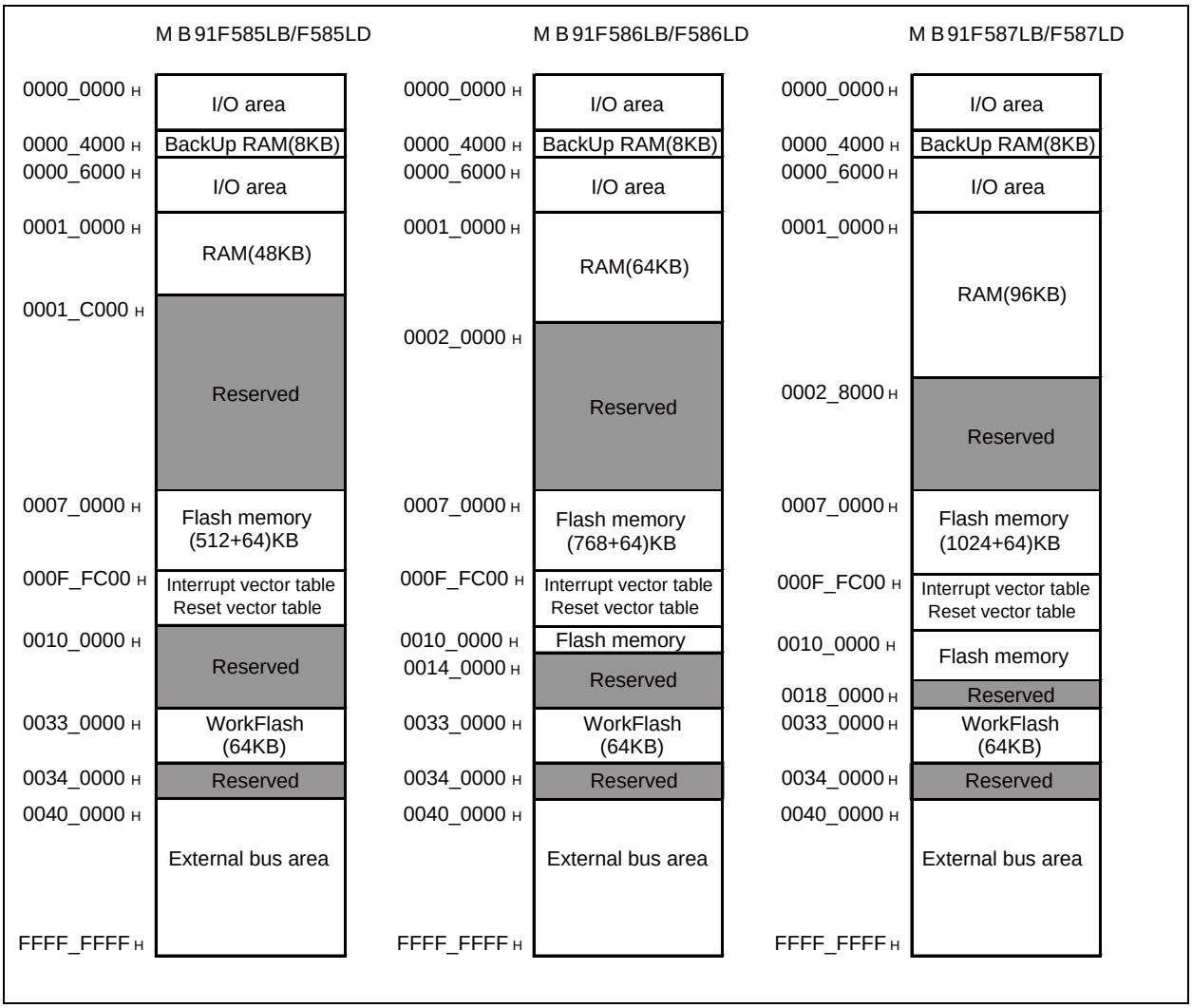


9. Memory Map

MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



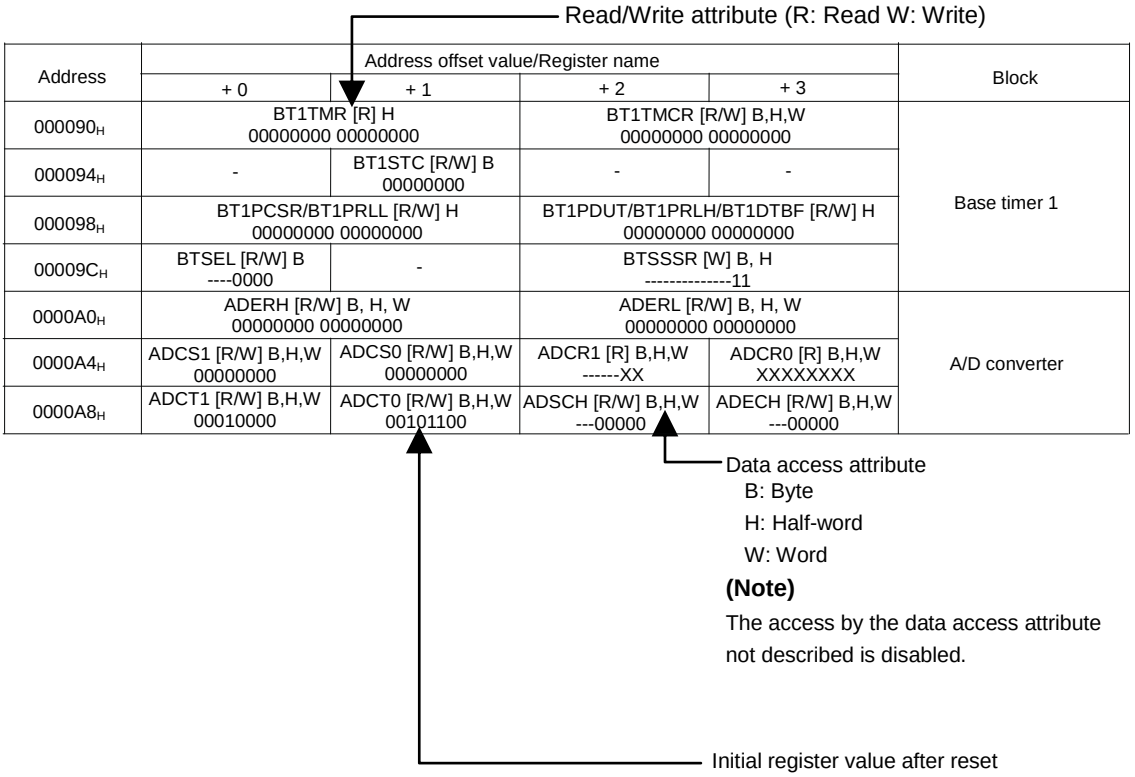
MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD



10. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

Legend of I/O Map



Address	Address offset value/Register name				Block
	+ 0	+ 1	+ 2	+ 3	
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] B,H,W 00000000 00000000		Base timer 1
000094_H	-	BT1STC [R/W] B 00000000	-	-	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL [R/W] B ----0000	-	BTSSSR [W] B, H ----------11		
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B,H,W 00000000	ADCS0 [R/W] B,H,W 00000000	ADCR1 [R] B,H,W ------XX	ADCR0 [R] B,H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B,H,W 00010000	ADCT0 [R/W] B,H,W 00101100	ADSCH [R/W] B,H,W ---00000	ADECH [R/W] B,H,W ---00000	

The initial register values after reset are indicated as follows:

"1": Initial value "1"

"0": Initial value "0"

"X": Initial value undefined

"-": Reserved bit/Undefined bit

"*": Initial value "0" or "1" according to the setting

Note:

It is prohibited to access addresses not described here.

MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W -----XXX	-	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008_H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXXX	-	-	
000010_H | 000038_H	-	-	-	-	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	-	-	-		Reserved
000044_H	DICR[R/W] B -------0	-	-	-	Delay interrupt
000048_H | $00005C_H$	-		-		Reserved
000060_H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068_H | $00007C_H$	-	-	-	-	Reserved
000080_H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084_H	BT0TMCR2[R/W] B -------0	BT0STC[R/W] B -0-0-0-0	-	-	
000088_H	BT0PCSR/BT0PRLL[R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	-	-	-	-	
000090_H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094_H	BT1TMCR2[R/W] B -------0	BT1STC[R/W] B -0-0-0-0	-	-	
000098_H	BT1PCSR/BT1PRLL[R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00009C$_H$	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -------- ------11		Base timer 0,1
0000A0$_H$ | 0000FC$_H$	-	-	-	-	Reserved
000100$_H$	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104$_H$	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108$_H$	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
00010C$_H$	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110$_H$	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114$_H$	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118$_H$ | 00011C$_H$	-	-	-	-	Reserved
000120$_H$	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124$_H$	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128$_H$	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
00012C$_H$	IRPR6H[R] B,H,W 000000--	IRPR6L[R] B,H,W 000000--	IRPR7H[R] B,H,W 000000--	IRPR7L[R] B,H,W 000000--	
000130$_H$	IRPR8H[R] B,H,W 000000--	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134$_H$	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138$_H$	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 00000000	IRPR13L[R] B,H,W 00000000	
00013C$_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 00000---	
000140 $_H$	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W 00------	IRPR17H[R] B,H,W 00------	IRPR17L[R]B,H,W 00------	
000144 $_H$	IRPR18H[R] B,H,W 00------	IRPR18L[R] B,H,W 000000--	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000148_H | $0001FC_H$	-	-	-	-	Reserved
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
$00020C_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210_H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214_H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		
000218_H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
$00021C_H$	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		
000220_H	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		PPG4
000224_H	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		
000228_H	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		PPG5
$00022C_H$	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		
000230_H	PCN6[R/W] B,H,W 00000000 000000-0		PCSR6[W] H,W XXXXXXXX XXXXXXXX		PPG6
000234_H	PDUT6[W] H,W XXXXXXXX XXXXXXXX		PTMR6[R] H,W 11111111 11111111		
000238_H	PCN7[R/W] B,H,W 00000000 000000-0		PCSR7[W] H,W XXXXXXXX XXXXXXXX		PPG7
$00023C_H$	PDUT7[W] H,W XXXXXXXX XXXXXXXX		PTMR7[R] H,W 11111111 11111111		
000240_H	PCN8[R/W] B,H,W 00000000 000000-0		PCSR8[W] H,W XXXXXXXX XXXXXXXX		PPG8
000244_H	PDUT8[W] H,W XXXXXXXX XXXXXXXX		PTMR8[R] H,W 11111111 11111111		
000248_H	PCN9[R/W] B,H,W 00000000 000000-0		PCSR9[W] H,W XXXXXXXX XXXXXXXX		PPG9
$00024C_H$	PDUT9[W] H,W XXXXXXXX XXXXXXXX		PTMR9[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000250_H	PCN10[R/W] B,H,W 00000000 000000-0		PCSR10[W] H,W XXXXXXXX XXXXXXXX		PPG10
000254_H	PDUT10[W] H,W XXXXXXXX XXXXXXXX		PTMR10[R] H,W 11111111 11111111		
000258_H	PCN11[R/W] B,H,W 00000000 000000-0		PCSR11[W] H,W XXXXXXXX XXXXXXXX		PPG11
$00025C_H$	PDUT11[W] H,W XXXXXXXX XXXXXXXX		PTMR11[R] H,W 11111111 11111111		
000260_H	PCN12[R/W] B,H,W 00000000 000000-0		PCSR12[W] H,W XXXXXXXX XXXXXXXX		PPG12
000264_H	PDUT12[W] H,W XXXXXXXX XXXXXXXX		PTMR12[R] H,W 11111111 11111111		
000268_H	PCN13[R/W] B,H,W 00000000 000000-0		PCSR13[W] H,W XXXXXXXX XXXXXXXX		PPG13
$00026C_H$	PDUT13[W] H,W XXXXXXXX XXXXXXXX		PTMR13[R] H,W 11111111 11111111		
000270_H	PCN14[R/W] B,H,W 00000000 000000-0		PCSR14[W] H,W XXXXXXXX XXXXXXXX		PPG14
000274_H	PDUT14[W] H,W XXXXXXXX XXXXXXXX		PTMR14[R] H,W 11111111 11111111		
000278_H	PCN15[R/W] B,H,W 00000000 000000-0		PCSR15[W] H,W XXXXXXXX XXXXXXXX		PPG15
$00027C_H$	PDUT15[W] H,W XXXXXXXX XXXXXXXX		PTMR15[R] H,W 11111111 11111111		
000280_H	PCN16[R/W] B,H,W 00000000 000000-0		PCSR16[W] H,W XXXXXXXX XXXXXXXX		PPG16
000284_H	PDUT16[W] H,W XXXXXXXX XXXXXXXX		PTMR16[R] H,W 11111111 11111111		
000288_H	PCN17[R/W] B,H,W 00000000 000000-0		PCSR17[W] H,W XXXXXXXX XXXXXXXX		PPG17
$00028C_H$	PDUT17[W] H,W XXXXXXXX XXXXXXXX		PTMR17[R] H,W 11111111 11111111		
000290_H	PCN18[R/W] B,H,W 00000000 000000-0		PCSR18[W] H,W XXXXXXXX XXXXXXXX		PPG18
000294_H	PDUT18[W] H,W XXXXXXXX XXXXXXXX		PTMR18[R] H,W 11111111 11111111		
000298_H	PCN19[R/W] B,H,W 00000000 000000-0		PCSR19[W] H,W XXXXXXXX XXXXXXXX		PPG19
$00029C_H$	PDUT19[W] H,W XXXXXXXX XXXXXXXX		PTMR19[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002A0_H$	PCN20[R/W] B,H,W 00000000 000000-0		PCSR20[W] H,W XXXXXXXX XXXXXXXX		PPG20
$0002A4_H$	PDUT20[W] H,W XXXXXXXX XXXXXXXX		PTMR20[R] H,W 11111111 11111111		
$0002A8_H$	PCN21[R/W] B,H,W 00000000 000000-0		PCSR21[W] H,W XXXXXXXX XXXXXXXX		PPG21
$0002AC_H$	PDUT21[W] H,W XXXXXXXX XXXXXXXX		PTMR21[R] H,W 11111111 11111111		
$0002B0_H$	PCN22[R/W] B,H,W 00000000 000000-0		PCSR22[W] H,W XXXXXXXX XXXXXXXX		PPG22
$0002B4_H$	PDUT22[W] H,W XXXXXXXX XXXXXXXX		PTMR22[R] H,W 11111111 11111111		
$0002B8_H$	PCN23[R/W] B,H,W 00000000 000000-0		PCSR23[W] H,W XXXXXXXX XXXXXXXX		PPG23
$0002BC_H$	PDUT23[W] H,W XXXXXXXX XXXXXXXX		PTMR23[R] H,W 11111111 11111111		
$0002C0_H$	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
$0002C4_H$	GTRS2[R/W] B,H,W -0000000 -0000000		GTRS3[R/W] B,H,W -0000000 -0000000		
$0002C8_H$	GTRS4[R/W] B,H,W -0000000 -0000000		GTRS5[R/W] B,H,W -0000000 -0000000		
$0002CC_H$	GTRS6[R/W] B,H,W -0000000 -0000000		GTRS7[R/W] B,H,W -0000000 -0000000		
$0002D0_H$	GTRS8[R/W] B,H,W -0000000 -0000000		GTRS9[R/W] B,H,W -0000000 -0000000		
$0002D4_H$	GTRS10[R/W] B,H,W -0000000 -0000000		GTRS11[R/W] B,H,W -0000000 -0000000		
$0002D8_H$	GTREN0[R/W] H,W 00000000 00000000		GTREN1[R/W] H,W -------- 00000000		
$0002DC_H$	-		-		Reserved
$0002E0_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
$0002E4_H$	-	GATEC4[R/W] B,H,W ------00	-	GATEC8[R/W] B,H,W ------00	
$0002E8_H$	-	GATEC10[R/W] B,H,W ------00	-	GATEC12[R/W] B,H,W ------00	
$0002EC_H$	-	-	-	-	Reserved
$0002F0_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
$0002F4_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002F8_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
$0002FC_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		MPU [S] (Only the CPU can access this area)
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clearing of DMA transfer requests
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W -----000	ICSEL11[R/W] B,H,W -----000	
$00040C_H$	ICSEL12[R/W] B,H,W -----000	ICSEL13[R/W] B,H,W -----000	ICSEL14[R/W] B,H,W -----000	ICSEL15[R/W] B,H,W -------0	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	
000414_H	ICSEL20[R/W] B,H,W -------0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	Generation and clearing of DMA transfer requests
000418_H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -------0	ICSEL27[R/W] B,H,W -------0	
$00041C_H$	-	-	-	-	
000420_H	-	-	-	-	
000424_H | $00043C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000440_H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444_H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448_H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
$00044C_H$	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450_H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454_H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458_H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
$00045C_H$	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460_H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464_H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468_H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
$00046C_H$	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470_H | $00047C_H$	-	-	-	-	Reserved [S]
000480_H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W* 000---11	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484_H	-	-	-	-	Reserved [S]
000488_H	DIVR0[R/W] B,H,W 000-----	-	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
$00048C_H$	-	-	-	-	Reserved [S]
000490_H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498_H	-	-	-	-	
$00049C_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0004A0_H$	-	-	-	-	Reserved
$0004A4_H$	CANPRE[R/W] B,H,W ----0000	-	-	-	CAN prescaler
$0004A8_H$ | $0004AC_H$	-	-	-	-	Reserved
$0004B0_H$	-	-	-	-	Reserved
$0004B4_H$ | $0004C0_H$	-	-	-	-	Reserved
$0004C4_H$	CUCR1[R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
$0004C8_H$	CUTR1[R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ | $0004DC_H$	-	-	-	-	Reserved
$0004E0_H$	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
$0004E4_H$	-	-	-	-	
$0004E8_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay/RDC clock control
$0004EC_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
$0004F0_H$ | $0004FC_H$	-	-	-	-	Reserved
000500_H	-				Reserved
000504_H	-				Reserved
000508_H | $00050C_H$	-	-	-	-	Reserved
000510_H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514_H	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00------	
000518_H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
$00051C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000520_H	CCPSSELR[R/W] B,H,W -------0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524_H	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528_H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] H,W 000----- --------		
$00052C_H$	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530_H	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534_H	-	-	-	-	
000538_H	-	-	-	-	
$00053C_H$	-	-	-	-	
000540_H | $00054C_H$	-	-	-	-	Reserved
000550_H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt (INT0 to 7)
000554_H | 000568_H	-	-	-	-	Reserved
$00056C_H$	-	CSVCR[R/W] B -0--1--0	-	-	CSV
000570_H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574_H | $00057C_H$	-	-	-	-	Reserved
000580_H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control
000584_H	LVD5R[R/W] B,H,W -------1	LVD5F[R/W] B,H,W 0-010--1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection
000588_H | $00058C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H | $00060C_H$	-	-	-	-	Reserved [S]
000610_H | $00063C_H$	-	-	-	-	Reserved [S]
000640_H | $00064C_H$	-	-	-	-	Reserved [S]
000650_H | $00067C_H$	-	-	-	-	Reserved [S]
000680_H | $00068C_H$	-	-	-	-	Reserved [S]
000690_H | $0006BC_H$	-	-	-	-	Reserved [S]
$0006C0_H$ | $0006CC_H$	-	-	-	-	Reserved [S]
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720_H | $0007F8_H$	-	-	-	-	Reserved
$0007FC_H$	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode
000800_H | $00083C_H$	-	-	-	-	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844_H	-	-	-	-	Reserved [S]
000848_H | 000854_H	-	-	-	-	Reserved [S]
000858_H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ | $00087C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0008C8_H$	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
$0008CC_H$	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008F4_H$	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F8_H$	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008FC_H$	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900_H | $000BF8_H$	-	-	-	-	Reserved
$000BFC_H$	-	-	UER[W] B,H,W -------- -------X		OCDU

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C00_H$	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
$000C04_H$	DCSR0[R/W] H 0------- -----000		DTCR0[R/W] H 00000000 00000000		
$000C08_H$	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1[R/W] H 0------- -----000		DTCR1[R/W] H 00000000 00000000		
$000C18_H$	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2[R/W] H 0------- -----000		DTCR2[R/W] H 00000000 00000000		
$000C28_H$	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
$000C38_H$	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		
$000C48_H$	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		DMA controller [S]
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ | $000DF0_H$	-	-	-	-	
$000DF4_H$	-	-	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	-	-	-	-	Reserved [S]
$000E00_H$	DDR00[R/W] B,H 00000000	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H -----000	-	DDR06[R/W] B,H 00000000	DDR07[R/W] B,H 00000000	
$000E08_H$	DDR08[R/W] B,H 00000000	DDR09[R/W] B,H 00000000	DDR10[R/W] B,H 00000000	DDR11[R/W] B,H 00000000	
$000E0C_H$	DDR12[R/W] B,H 00000000	DDR13[R/W] B,H 00-00000	-	-	
$000E10_H$ | $000E1C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E20_H$	PFR00[R/W] B,H 00000000	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H -----000	-	PFR06[R/W] B,H 00000000	PFR07[R/W] B,H 00000000	
$000E28_H$	PFR08[R/W] B,H 00000000	PFR09[R/W] B,H 00000000	PFR10[R/W] B,H 00000000	PFR11[R/W] B,H 00000000	
$000E2C_H$	PFR12[R/W] B,H 00000000	PFR13[R/W] B,H 00-00000	-	-	
$000E30_H$ | $000E3C_H$	-	-	-	-	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W -----XXX	-	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	-	-	
$000E50_H$ | $000E5C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E60_H$	EPFR00[R/W] B,H -----000	EPFR01[R/W] B,H ------00	EPFR02[R/W] B,H --000000	EPFR03[R/W] B,H 00000000	Extended port function register
$000E64_H$	EPFR04[R/W] B,H 00000000	EPFR05[R/W] B,H 00000000	EPFR06[R/W] B,H ------00	EPFR07[R/W] B,H ----0000	
$000E68_H$	EPFR08[R/W] B,H ----0000	EPFR09[R/W] B,H -------0	EPFR10[R/W] B,H 00000000	EPFR11[R/W] B,H ----0000	
$000E6C_H$	EPFR12[R/W] B,H --000000	EPFR13[R/W] B,H -------1	EPFR14[R/W] B,H -0000000	EPFR15[R/W] B,H -0000000	
$000E70_H$	EPFR16[R/W] B,H --000000	EPFR17[R/W] B,H 00000000	EPFR18[R/W] B,H 00000000	EPFR19[R/W] B,H 00000000	
$000E74_H$	EPFR20[R/W] B,H 00000000	EPFR21[R/W] B,H 00000000	EPFR22[R/W] B,H 00000000	EPFR23[R/W] B,H 00000000	
$000E78_H$	EPFR24[R/W] B,H 00000000	EPFR25[R/W] B,H 00000000	EPFR26[R/W] B,H 00000000	EPFR27[R/W] B,H 00000000	
$000E7C_H$	EPFR28[R/W] B,H 00000000	EPFR29[R/W] B,H 00000000	EPFR30[R/W] B,H 00000000	EPFR31[R/W] B,H 00000000	
$000E80_H$	EPFR32[R/W] B,H 00000000	-	-	-	
$000E84_H$ | $000EBC_H$	-	-	-	-	Reserved
$000EC0_H$	PPER00[R/W] B,H 00000000	PPER01[R/W] B,H 00000000	PPER02[R/W] B,H 00000000	PPER03[R/W] B,H 00000000	Port pull-up/down enable register
$000EC4_H$	PPER04[R/W] B,H -----000	-	PPER06[R/W] B,H 00000000	PPER07[R/W] B,H 00000000	
$000EC8_H$	PPER08[R/W] B,H 00000000	PPER09[R/W] B,H 00000000	PPER10[R/W] B,H 00000000	PPER11[R/W] B,H 00000000	
$000ECC_H$	PPER12[R/W] B,H 00000000	PPER13[R/W] B,H 00-00000	-	-	
$000ED0_H$ | $000EDC_H$	-	-	-	-	Reserved
$000EE0_H$	PILR00[R/W] B,H 11111111	PILR01[R/W] B,H 11111111	PILR02[R/W] B,H 11111111	PILR03[R/W] B,H 11111111	Port input level selection register
$000EE4_H$	PILR04[R/W] B,H -----111	-	PILR06[R/W] B,H 11111111	PILR07[R/W] B,H 11111111	
$000EE8_H$	PILR08[R/W] B,H 11111111	PILR09[R/W] B,H 11111111	PILR10[R/W] B,H 11111111	PILR11[R/W] B,H 11111111	
$000EEC_H$	PILR12[R/W] B,H 11111111	PILR13[R/W] B,H 11-11111	-	-	
$000EF0_H$ | $000EFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000F00_H$ | $000F1C_H$	-	-	-	-	Reserved
$000F20_H$	PODR00[R/W] B,H 00000000	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
$000F24_H$	PODR04[R/W] B,H -----000	-	PODR06[R/W] B,H 00000000	PODR07[R/W] B,H 00000000	
$000F28_H$	PODR08[R/W] B,H 00000000	PODR09[R/W] B,H 00000000	PODR10[R/W] B,H 00000000	PODR11[R/W] B,H 00000000	
$000F2C_H$	PODR12[R/W] B,H 00000000	PODR13[R/W] B,H 00-00000	-	-	
$000F30_H$ | $000F3C_H$	-	-	-	-	Reserved
$000F40_H$	PORTEN[R/W] B,H,W ------00	-	-	-	Port input enable register
$000F44_H$	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
$000F48_H$	ADERH[R/W] B,H -------- 11111111		ADERL[R/W] B,H 11111111 11111111		Analog input enable register
$000F4C_H$	-	-	-	-	Reserved
$000F50_H$ | $000FFC_H$	-	-	-	-	Reserved
001000_H	SACR[R/W] B,H,W -------0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asynchronous switch control
001004_H | $0010BC_H$	-	-	-	-	Reserved
$0010C0_H$	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation
$0010C4_H$	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
$0010C8_H$	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
$0010CC_H$	CRCR[R] B,H,W 11111111 11111111 11111111 11111111				
$0010D0_H$ | $0010FC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001100_H	TCGS[R/W] B,H,W ------00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104_H	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108_H	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00110C_H$	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110_H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 --------				
001114_H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118_H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00111C_H$	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120_H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 --------				
001124_H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128_H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00112C_H$	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130_H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 --------				
001134_H	FRS0[R/W] B,H,W -------- -000-000 -000-000 -000-000				Free-run timer selection
001138_H	FRS1[R/W] B,H,W -------- -------- -000-000 -000-000				
$00113C_H$	FRS2[R/W] B,H,W -------- -000-000 -000-000 -000-000				
001140_H	FRS3[R/W] B,H,W -------- -------- -000-000 -000-000				
001144_H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148_H	FRS5[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
$00114C_H$	FRS6[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001150_H	-				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001154_H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158_H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W ------00	
$00115C_H$	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160_H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W ------00	
001164_H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168_H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W ------00	
$00116C_H$	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170_H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W ------00	
001174_H	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178_H	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W ------00	
$00117C_H$	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180_H	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W ------00	
001184_H	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188_H	ICS01[R/W] B,H,W ------00 00000000		-	LSYNS[R/W] B,H,W ---00000	
$00118C_H$	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190_H	ICS23[R/W] B,H,W ------00 00000000		-	-	
001194_H	IPCP4[R] H,W 00000000 00000000		IPCP5[R] H,W 00000000 00000000		Input capture 4/5
001198_H	ICS45[R/W] B,H,W ------00 00000000		-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00119C$_H$	IPCP6[R] H,W 00000000 00000000		IPCP7[R] H,W 00000000 00000000		Input capture 6/7
0011A0$_H$	ICS67[R/W] B,H,W ------00 00000000		-	-	
0011A4$_H$	DTSR[R/W] B,H,W ------10	-	-	-	DTTI selection
0011A8$_H$	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0011AC$_H$	TMRR2[R/W] H,W 00000000 00000001		-	-	
0011B0$_H$	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
0011B4$_H$	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
0011B8$_H$	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
0011BC$_H$	PICS0[R/W] B,H,W 000000-- -------- -------- --------				
0011C0$_H$	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
0011C4$_H$	TMRR5[R/W] H,W 00000000 00000001		-	-	
0011C8$_H$	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
0011CC$_H$	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00---000	
0011D0$_H$	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W 000000-1	
0011D4$_H$	PICS1[R/W] B,H,W 000000-- -------- -------- --------				
0011D8$_H$	-	-	-	-	12-bit A/D converter
0011DC$_H$	ADTSS[R/W] B,H,W -------0	-	-	-	
0011E0$_H$	ADTSE[R/W] B,H,W -------- 00000000 00000000 00000000				
0011E4$_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
0011E8$_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
0011EC$_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0011F0_H$	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		12-bit A/D converter
$0011F4_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
$0011F8_H$	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
$0011FC_H$	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001200_H	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
001204_H	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001208_H	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
$00120C_H$	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001210_H	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
001214_H	-	-	-	-	
001218_H	-	-	-	-	
$00121C_H$	-	-	-	-	
001220_H	-	-	-	-	
001224_H	ADTCS0[R/W] B,H,W 00000000 0010-000		ADTCS1[R/W] B,H,W 00000000 0010-000		
001228_H	ADTCS2[R/W] B,H,W 00000000 0010-000		ADTCS3[R/W] B,H,W 00000000 0010-000		
$00122C_H$	ADTCS4[R/W] B,H,W 00000000 0010-000		ADTCS5[R/W] B,H,W 00000000 0010-000		
001230_H	ADTCS6[R/W] B,H,W 00000000 0010-000		ADTCS7[R/W] B,H,W 00000000 0010-000		
001234_H	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		
001238_H	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
$00123C_H$	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240_H	ADTCS14[R/W] B,H,W 00000000 0010-000		ADTCS15[R/W] B,H,W 00000000 0010-000		
001244_H	ADTCS16[R/W] B,H,W 00000000 00100000		ADTCS17[R/W] B,H,W 00000000 00100000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001248_H	ADTCS18[R/W] B,H,W 00000000 00100000		ADTCS19[R/W] B,H,W 00000000 00100000		12-bit A/D converter
$00124C_H$	ADTCS20[R/W] B,H,W 00000000 00100000		ADTCS21[R/W] B,H,W 00000000 00100000		
001250_H	ADTCS22[R/W] B,H,W 00000000 00100000		ADTCS23[R/W] B,H,W 00000000 00100000		
001254_H	-	-	-	-	
001258_H	-	-	-	-	
$00125C_H$	-	-	-	-	
001260_H	-	-	-	-	
001264_H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268_H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
$00126C_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274_H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278_H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$00127C_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280_H	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
001284_H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
001288_H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		
$00128C_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		
001290_H	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
001294_H	-	-	-	-	
001298_H	-	-	-	-	
$00129C_H$	-	-	-	-	
$0012A0_H$	-	-	-	-	
$0012A4_H$	ADCS0[R/W] B,H,W 0------- --------		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0012A8$_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	12-bit A/D converter
0012AC$_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
0012B0$_H$ | 0012FC$_H$	-	-	-	-	Reserved
001300$_H$	RDCCTR0[R/W] B,H,W 0----000	RDCCTR1[R/W] B,H,W -0000000	RDCINTR[R] B,H,W -0000000	RDCICER[R/W] B,H,W ------00	RDC
001304$_H$	-	RDCCTR2[R/W] B,H,W ---00000	RDCIPR[R/W] H,W ----0000 00000000		
001308$_H$	RDCCPR1[R/W] H,W ----0000 00000000		RDCCPR2[R/W] H,W ----0000 00000000		
00130C$_H$	RDCCPR3[R/W] H,W ------00 00000000		RDCCPR4[R/W] H,W ------00 00000000		
001310$_H$	AGLDR[R] H,W 1---XXXX XXXXXXXX		AGVLDR[R] H,W XXXXXXXX XXXXXXXX		
001314$_H$	AGLDBR[R] H,W 1---XXXX XXXXXXXX		AGVLDBR[R] H,W XXXXXXXX XXXXXXXX		
001318 $_H$	SCCIR[R/W] H,W 1---0000 00000000		-	-	
00131C$_H$	SINDR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001320$_H$	COSDR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				RDC
001324$_H$	-		-		
001328$_H$	SINDR1[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00132C$_H$	COSDR1[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001330$_H$	-		-		
001334$_H$ | 0013FC$_H$	-	-	-	-	Reserved
001400$_H$	-	-	-	-	Reserved
001404$_H$ | 0014FC$_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001500_H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0[R/W] B,H,W 000000-0	SSR0[R/W] B,H,W 0--00011	ESCR0/(IBSR0) [R/W] B,H,W 00000000	Multi Function Serial I/F 0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001504_H	-/(RDR10/(TDR10))[R/W] H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001508_H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
$00150C_H$	STMCR0[R/W] B,H,W 00000000 00000000		-/(SFUR0) [R/W] B,H,W -------- -------- *4		
001510_H	-	-	-/(SFLR10) [R/W] B,H,W -------- *4	-/(SFLR00) [R/W] B,H,W -------- *4	
001514_H	-	-	-	-	
001518_H	-	-	-	-	
$00151C_H$	BGR0[R/W] H,W 00000000 00000000		-/(ISMK0)[R/W] B,H,W -------- *2	-/(ISBA0)[R/W] B,H,W -------- *2	
001520_H	FCR10[R/W] B,H,W 00-00100	FCR00[R/W] B,H,W -0000000	FBYTE20[R/W] B,H,W 00000000	FBYTE10[R/W] B,H,W 00000000	
001524_H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1/(IBSR1) [R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528_H	-/(RDR11/(TDR11))[R/W] H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
$00152C_H$	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530_H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W -------- -------- *3,*4		
001534_H	-/(SCSTR31) [R/W] B,H,W -------- *3	-/(SCSTR21) [R/W] B,H,W -------- *3	-/(SCSTR11/SFLR11) [R/W] B,H,W -------- *3,*4	-/(SCSTR01/SFLR01) [R/W] B,H,W -------- *3,*4	
001538_H	-	-	-	-	
$00153C_H$	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540_H	BGR1[R/W] H,W 00000000 00000000		-/(ISMK1)[R/W] B,H,W -------- *2	-/(ISBA1)[R/W] B,H,W -------- *2	
001544_H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001548$_H$	SCR2[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000000-0	SSR2[R/W] B,H,W 0--00011	ESCR2[R/W] B,H,W 00000000	Multi Function Serial I/F 2 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
00154C$_H$	-/(RDR12/(TDR12))[R/W] H,W -------- -------- *3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1		
001550$_H$	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
001554$_H$	STMCR2[R/W] B,H,W 00000000 00000000		-/(SCSCR2/SFUR2) [R/W] B,H,W -------- -------- *3,*4		
001558$_H$	-/(SCSTR32) [R/W] B,H,W -------- *3	-/(SCSTR22) [R/W] B,H,W -------- *3	-/(SCSTR12/SFLR12) [R/W] B,H,W -------- *3,*4	-/(SCSTR02/SFLR02) [R/W] B,H,W -------- *3,*4	
00155C$_H$	-	-	-	-	
001560$_H$	-	-	-	TBYTE02[R/W] B,H,W 00000000	
001564$_H$	BGR2[R/W] H,W 00000000 00000000		-	-	
001568$_H$	FCR12[R/W] B,H,W 00-00100	FCR02[R/W] B,H,W -0000000	FBYTE22[R/W] B,H,W 00000000	FBYTE12[R/W] B,H,W 00000000	
00156C$_H$	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000000-0	SSR3[R/W] B,H,W 0--00011	ESCR3/(IBSR3) [R/W] B,H,W 00000000	Multi Function Serial I/F 3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^{2}C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001570$_H$	-/(RDR13/(TDR13))[R/W] H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
001574$_H$	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
001578$_H$	STMCR3[R/W] B,H,W 00000000 00000000		-/(SCSCR3/SFUR3) [R/W] B,H,W -------- -------- *3,*4		
00157C$_H$	-/(SCSTR33) [R/W] B,H,W -------- *3	-/(SCSTR23) [R/W] B,H,W -------- *3	-/(SCSTR13/SFLR13) [R/W] B,H,W -------- *3,*4	-/(SCSTR03/SFLR03) [R/W] B,H,W -------- *3,*4	
001580$_H$	-	-	-	-	
001584$_H$	-	-	-	TBYTE03[R/W] B,H,W 00000000	
001588$_H$	BGR3[R/W] H,W 00000000 00000000		-/(ISMK3)[R/W] B,H,W -------- *2	-/(ISBA3)[R/W] B,H,W -------- *2	
00158C$_H$	FCR13[R/W] B,H,W 00-00100	FCR03[R/W] B,H,W -0000000	FBYTE23[R/W] B,H,W 00000000	FBYTE13[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001590_H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000000-0	SSR4[R/W] B,H,W 0--00011	ESCR4/(IBSR4) [R/W] B,H,W 00000000	Multi Function Serial I/F 4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001594_H	-/(RDR14/(TDR14))[R/W] H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
001598_H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
$00159C_H$	STMCR4[R/W] B,H,W 00000000 00000000		-/(SCSCR4/SFUR4) [R/W] B,H,W -------- -------- *3,*4		
$0015A0_H$	-/(SCSTR34) [R/W] B,H,W -------- *3	-/(SCSTR24) [R/W] B,H,W -------- *3	-/(SCSTR14/SFLR14) [R/W] B,H,W -------- *3,*4	-/(SCSTR04/SFLR04) [R/W] B,H,W -------- *3,*4	
$0015A4_H$	-	-/(SCSFR24)[R/W] B,H,W -------- *3	-/(SCSFR14)[R/W] B,H,W -------- *3	-/(SCSFR04)[R/W] B,H,W -------- *3	
$0015A8_H$	-/(TBYTE34)[R/W] B,H,W -------- *3	-/(TBYTE24)[R/W] B,H,W -------- *3	-/(TBYTE14)[R/W] B,H,W -------- *3	TBYTE04[R/W] B,H,W 00000000	
$0015AC_H$	BGR4[R/W] H,W 00000000 00000000		-/(ISMK4)[R/W] B,H,W -------- *2	-/(ISBA4)[R/W] B,H,W -------- *2	
$0015B0_H$	FCR14[R/W] B,H,W 00-00100	FCR04[R/W] B,H,W -0000000	FBYTE24[R/W] B,H,W 00000000	FBYTE14[R/W] B,H,W 00000000	
$0015B4_H$ | $001FFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002000_H	CTRLR0[R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN 0 64msb
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008_H	INTR0[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0[R/W] B,H,W -------- ----0000		-		
002010_H	IF1CREQ0[R/W] B,H,W 0------- 00000001		IF1CMSK0[R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
$00201C_H$	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020_H	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		
002028_H, $00202C_H$	-		-		
002030_H, 002034_H	Reserved (IF1 data mirror)				
002038_H, $00203C_H$	-		-		
002040_H	IF2CREQ0[R/W] B,H,W 0------- 00000001		IF2CMSK0[R/W] B,H,W -------- 00000000		
002044_H	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		
002048_H	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_H	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
002058_H, $00205C_H$	-		-		
002060_H, 002064_H	Reserved (IF2 data mirror)				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002068_H | $00207C_H$	-		-		CAN 0 64msb
002080_H	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_H	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_H	-		-		
$00208C_H$	-		-		
002090_H	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_H	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098_H	-		-		
$00209C_H$	-		-		
$0020A0_H$	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
$0020A4_H$	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
$0020A8_H$	-		-		
$0020AC_H$	-		-		
$0020B0_H$	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
$0020B8_H$	-		-		
$0020BC_H$	-		-		
$0020C0_H$ | $0020FC_H$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002100_H	CTRLR1[R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN 1 64msb
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108_H	INTR1[R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1[R/W] B,H,W -------- ----0000		-		
002110_H	IF1CREQ1[R/W] B,H,W 0------- 00000001		IF1CMSK1[R/W] B,H,W -------- 00000000		
002114_H	IF1MSK21[R/W] B,H,W 11-11111 11111111		IF1MSK11[R/W] B,H,W 11111111 11111111		
002118_H	IF1ARB21[R/W] B,H,W 00000000 00000000		IF1ARB11[R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1[R/W] B,H,W 00000000 0---0000		-		
002120_H	IF1DTA11[R/W] B,H,W 00000000 00000000		IF1DTA21[R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11[R/W] B,H,W 00000000 00000000		IF1DTB21[R/W] B,H,W 00000000 00000000		
002128_H, $00212C_H$	-		-		
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H, $00213C_H$	-		-		
002140_H	IF2CREQ1[R/W] B,H,W 0------- 00000001		IF2CMSK1[R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21[R/W] B,H,W 11-11111 11111111		IF2MSK11[R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21[R/W] B,H,W 00000000 00000000		IF2ARB11[R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1[R/W] B,H,W 00000000 0---0000		-		
002150_H	IF2DTA11[R/W] B,H,W 00000000 00000000		IF2DTA21[R/W] B,H,W 00000000 00000000		
002154_H	IF2DTB11[R/W] B,H,W 00000000 00000000		IF2DTB21[R/W] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002158_{H,}$ $00215C_{H}$	-		-		CAN 1 64msb
$002160_{H,}$ 002164_{H}	Reserved (IF2 data mirror)				
002168_{H} | $00217C_{H}$	-		-		
002180_{H}	TREQR21[R] B,H,W 00000000 00000000		TREQR11[R] B,H,W 00000000 00000000		
002184_{H}	TREQR41[R] B,H,W 00000000 00000000		TREQR31[R] B,H,W 00000000 00000000		
002188_{H}	-		-		
$00218C_{H}$	-		-		
002190_{H}	NEWDT21[R] B,H,W 00000000 00000000		NEWDT11[R] B,H,W 00000000 00000000		
002194_{H}	NEWDT41[R] B,H,W 00000000 00000000		NEWDT31[R] B,H,W 00000000 00000000		
002198_{H}	-		-		
$00219C_{H}$	-		-		
$0021A0_{H}$	INTPND21[R] B,H,W 00000000 00000000		INTPND11[R] B,H,W 00000000 00000000		
$0021A4_{H}$	INTPND41[R] B,H,W 00000000 00000000		INTPND31[R] B,H,W 00000000 00000000		
$0021A8_{H}$	-		-		
$0021AC_{H}$	-		-		
$0021B0_{H}$	MSGVAL21[R] B,H,W 00000000 00000000		MSGVAL11[R] B,H,W 00000000 00000000		
$0021B4_{H}$	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		
$0021B8_{H}$	-		-		
$0021BC_{H}$	-		-		
$0021C0_{H}$ | $0021FC_{H}$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002200_H	CTRLR2[R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN 2 64msb
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208_H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2[R/W] B,H,W -------- ----0000		-		
002210_H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22[R/W] B,H,W 11-11111 11111111		IF1MSK12[R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22[R/W] B,H,W 00000000 00000000		IF1ARB12[R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2[R/W] B,H,W 00000000 0---0000		-		
002220_H	IF1DTA12[R/W] B,H,W 00000000 00000000		IF1DTA22[R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12[R/W] B,H,W 00000000 00000000		IF1DTB22[R/W] B,H,W 00000000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002228_{H,}$ $00222C_{H}$	-		-		CAN 2 64msb
$002230_{H,}$ 002234_{H}	Reserved (IF1 data mirror)				
$002238_{H,}$ $00223C_{H}$	-		-		
002240_{H}	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_{H}	IF2MSK22[R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_{H}	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_{H}$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		-		
002250_{H}	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_{H}	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
$002258_{H,}$ $00225C_{H}$	-		-		
$002260_{H,}$ 002264_{H}	Reserved (IF2 data mirror)				
002268_{H} | $00227C_{H}$	-		-		
002280_{H}	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284_{H}	TREQR42[R] B,H,W 00000000 00000000		TREQR32[R] B,H,W 00000000 00000000		
002288_{H}	-		-		
$00228C_{H}$	-		-		
002290_{H}	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294_{H}	NEWDT42[R] B,H,W 00000000 00000000		NEWDT32[R] B,H,W 00000000 00000000		
002298_{H}	-		-		
$00229C_{H}$	-		-		
$0022A0_{H}$	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
$0022A4_{H}$	INTPND42[R] B,H,W 00000000 00000000		INTPND32[R] B,H,W 00000000 00000000		
$0022A8_{H}$	-		-		
$0022AC_{H}$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0022B0_H$	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		CAN 2 64msb
$0022B4_H$	MSGVAL42[R] B,H,W 00000000 00000000		MSGVAL32[R] B,H,W 00000000 00000000		
$0022B8_H$	-		-		
$0022BC_H$	-		-		
$0022C0_H$ | $0022FC_H$	-	-	-	-	
002300_H	DFCTLR[R/W] B,H,W -0------ --------		-	DFSTR[R/W] B,H,W -----001	WorkFlash
002304_H	-	-	-	-	
002308_H	FLIFCTLR[R/W] B,H,W ---0--00	-	FLIFFER1[R/W] B,H,W --------	FLIFFER2[R/W] B,H,W --------	
$00230C_H$ | $002FFC_H$	-	-	-	-	Reserved
003000_H	SEEARX[R] B,H,W -0000000 00000000		DEEARX[R] B,H,W -0000000 00000000		XBS RAM ECC control register
003004_H	EECSRX[R/W] B,H,W ----00-0	-	EFEARX[R/W] B,H,W -0000000 00000000		
003008_H	-	EFECRX[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				XBS RAM diagnosis register
003010_H	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014_H	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018_H	TAEARX[R/W] B,H,W -1011111 11111111		TASARX[R/W] B,H,W -0000000 00000000		
$00301C_H$	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W ------00 00001100		
003020_H	TSRCRX[R/W] B,H,W 0-------	-	-	TKCCRX[R/W] B,H,W 00----00	
003024_H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028_H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
$00302C_H$	-	EFECRA[R/W] B,H,W -------0 00000000 00000000			

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				Backup RAM diagnosis register
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W ------00 00001100		
003044_H	TSRCRA[R/W] B,H,W 0-------	-	-	TKCCRA[R/W] B,H,W 00----00	
003048_H | $0030FC_H$	-	-	-	-	Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ | $00D07C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 --001110				
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD
$00D09C_H$	-				Reserved
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 --000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				
$00D0CC_H$ | $00D0FC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$ $00D10C_H$	-				Reserved
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W -------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	-				
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
$00D304_H$	FRF[R/W] W -------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				FlexRay MHD
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				
$00D33C_H$	NDAT4[R] W 00000000 00000000 00000000 00000000				
$00D340_H$	MBSC1[R] W 00000000 00000000 00000000 00000000				
$00D344_H$	MBSC2[R] W 00000000 00000000 00000000 00000000				
$00D348_H$	MBSC3[R] W 00000000 00000000 00000000 00000000				
$00D34C_H$	MBSC4[R] W 00000000 00000000 00000000 00000000				
$00D350_H$ | $00D3EC_H$	-				Reserved
$00D3F0_H$	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF
$00D3F4_H$	ENDN[R] W 10000111 01100101 01000011 00100001				
$00D3F8_H$ | $00D3FC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D400_H$ | $00D4FC_H$	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF
$00D500_H$	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
$00D504_H$	WRHS2[R/W] W -------- -0000000 -----000 00000000				
$00D508_H$	WRHS3[R/W] W -------- -------- -----000 00000000				
$00D50C_H$	-				
$00D510_H$	IBCM[R/W] W -------- ------00 -------- -----000				
$00D514_H$	IBCR[R/W] W 0------- -0000000 0------- -0000000				
$00D518_H$ | $00D5FC_H$	-				Reserved
$00D600_H$ | $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ | $00D7FC_H$	-				Reserved
$00D800_H$ | $00EFFC_H$	-				Reserved
$00F000_H$ | $00FEFC_H$	-				Reserved [S]
$00FF00_H$	DSUCR[R/W] B,H,W -------- -------0		-	-	OCDU [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00FF04_H$ | $00FF0C_H$	-	-	-	-	Reserved [S]
$00FF10_H$	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ | $00FFF4_H$	-	-	-	-	Reserved [S]
$00FFF8_H$	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]:It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000000_H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004_H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W XXXXXXXX	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008_H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
$00000C_H$	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXXX	-	-	
000010_H | 000038_H	-	-	-	-	Reserved
$00003C_H$	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0010	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040_H	-	-	-	-	Reserved
000044_H	DICR[R/W] B -------0	-	-	-	Delay interrupt
000048_H | $00005C_H$	-		-		Reserved
000060_H	TMRLRA0[R/W] H XXXXXXXX XXXXXXXX		TMR0[R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064_H	TMRLRB0[R/W] H XXXXXXXX XXXXXXXX		TMCSR0[R/W] B,H,W 00000000 0-000000		
000068_H | $00007C_H$	-	-	-	-	Reserved
000080_H	BT0TMR[R] H 00000000 00000000		BT0TMCR[R/W] H -0000000 00000000		Base timer 0
000084_H	BT0TMCR2 [R/W] B -------0	BT0STC [R/W] B -0-0-0-0	-	-	
000088_H	BT0PCSR/BT0PRLL [R/W] H 00000000 00000000		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H 00000000 00000000		
$00008C_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W] H -0000000 00000000		Base timer 1
000094_H	BT1TMCR2 [R/W] B -------0	BT1STC [R/W] B -0-0-0-0	-	-	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01[R/W] B ----0000	-	BTSSSR[W] B,H -------- ------11		Base timer 0, 1
$0000A0_H$ | $0000FC_H$	-	-	-	-	Reserved
000100_H	TMRLRA1[R/W] H XXXXXXXX XXXXXXXX		TMR1[R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104_H	TMRLRB1[R/W] H XXXXXXXX XXXXXXXX		TMCSR1[R/W] B,H,W 00000000 0-000000		
000108_H	TMRLRA2[R/W] H XXXXXXXX XXXXXXXX		TMR2[R] H XXXXXXXX XXXXXXXX		Reload timer 2
$00010C_H$	TMRLRB2[R/W] H XXXXXXXX XXXXXXXX		TMCSR2[R/W] B,H,W 00000000 0-000000		
000110_H	TMRLRA3[R/W] H XXXXXXXX XXXXXXXX		TMR3[R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114_H	TMRLRB3[R/W] H XXXXXXXX XXXXXXXX		TMCSR3[R/W] B,H,W 00000000 0-000000		
000118_H | $00011C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000120_H	IRPR0H[R] B,H,W 00------	IRPR0L[R] B,H,W 00------	IRPR1H[R] B,H,W 00------	IRPR1L[R] B,H,W --------	Interrupt request batch read register
000124_H	IRPR2H[R] B,H,W --------	IRPR2L[R] B,H,W 0000----	IRPR3H[R] B,H,W 00------	IRPR3L[R] B,H,W 00------	
000128_H	IRPR4H[R] B,H,W 00------	IRPR4L[R] B,H,W 000000--	IRPR5H[R] B,H,W 00------	IRPR5L[R] B,H,W 00------	
$00012C_H$	IRPR6H[R] B,H,W 000000--	IRPR6L[R] B,H,W 000000--	IRPR7H[R] B,H,W 000000--	IRPR7L[R] B,H,W 000000--	
000130_H	IRPR8H[R] B,H,W 000000--	IRPR8L[R] B,H,W 00------	IRPR9H[R] B,H,W 00------	IRPR9L[R] B,H,W 00------	
000134_H	IRPR10H[R] B,H,W 00------	IRPR10L[R] B,H,W 00------	IRPR11H[R] B,H,W 00------	IRPR11L[R] B,H,W 0000000-	
000138_H	IRPR12H[R] B,H,W 0000000-	IRPR12L[R] B,H,W 00000000	IRPR13H[R] B,H,W 00000000	IRPR13L[R] B,H,W 00000000	
$00013C_H$	IRPR14H[R] B,H,W 00------	IRPR14L[R] B,H,W 00------	IRPR15H[R] B,H,W 00000000	IRPR15L[R] B,H,W 00000---	
000140_H	IRPR16H[R] B,H,W 00------	IRPR16L[R] B,H,W 00------	IRPR17H[R] B,H,W 00------	IRPR17L[R] B,H,W 00------	
000144_H	IRPR18H[R] B,H,W 00------	IRPR18L[R] B,H,W 000000--	-	-	
000148_H | $0001FC_H$	-	-	-	-	Reserved
000200_H	PCN0[R/W] B,H,W 00000000 000000-0		PCSR0[W] H,W XXXXXXXX XXXXXXXX		PPG0
000204_H	PDUT0[W] H,W XXXXXXXX XXXXXXXX		PTMR0[R] H,W 11111111 11111111		
000208_H	PCN1[R/W] B,H,W 00000000 000000-0		PCSR1[W] H,W XXXXXXXX XXXXXXXX		PPG1
$00020C_H$	PDUT1[W] H,W XXXXXXXX XXXXXXXX		PTMR1[R] H,W 11111111 11111111		
000210_H	PCN2[R/W] B,H,W 00000000 000000-0		PCSR2[W] H,W XXXXXXXX XXXXXXXX		PPG2
000214_H	PDUT2[W] H,W XXXXXXXX XXXXXXXX		PTMR2[R] H,W 11111111 11111111		
000218_H	PCN3[R/W] B,H,W 00000000 000000-0		PCSR3[W] H,W XXXXXXXX XXXXXXXX		PPG3
$00021C_H$	PDUT3[W] H,W XXXXXXXX XXXXXXXX		PTMR3[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000220_H	PCN4[R/W] B,H,W 00000000 000000-0		PCSR4[W] H,W XXXXXXXX XXXXXXXX		PPG4
000224_H	PDUT4[W] H,W XXXXXXXX XXXXXXXX		PTMR4[R] H,W 11111111 11111111		
000228_H	PCN5[R/W] B,H,W 00000000 000000-0		PCSR5[W] H,W XXXXXXXX XXXXXXXX		PPG5
$00022C_H$	PDUT5[W] H,W XXXXXXXX XXXXXXXX		PTMR5[R] H,W 11111111 11111111		
000230_H	PCN6[R/W] B,H,W 00000000 000000-0		PCSR6[W] H,W XXXXXXXX XXXXXXXX		PPG6
000234_H	PDUT6[W] H,W XXXXXXXX XXXXXXXX		PTMR6[R] H,W 11111111 11111111		
000238_H	PCN7[R/W] B,H,W 00000000 000000-0		PCSR7[W] H,W XXXXXXXX XXXXXXXX		PPG7
$00023C_H$	PDUT7[W] H,W XXXXXXXX XXXXXXXX		PTMR7[R] H,W 11111111 11111111		
000240_H	PCN8[R/W] B,H,W 00000000 000000-0		PCSR8[W] H,W XXXXXXXX XXXXXXXX		PPG8
000244_H	PDUT8[W] H,W XXXXXXXX XXXXXXXX		PTMR8[R] H,W 11111111 11111111		
000248_H	PCN9[R/W] B,H,W 00000000 000000-0		PCSR9[W] H,W XXXXXXXX XXXXXXXX		PPG9
$00024C_H$	PDUT9[W] H,W XXXXXXXX XXXXXXXX		PTMR9[R] H,W 11111111 11111111		
000250_H	PCN10[R/W] B,H,W 00000000 000000-0		PCSR10[W] H,W XXXXXXXX XXXXXXXX		PPG10
000254_H	PDUT10[W] H,W XXXXXXXX XXXXXXXX		PTMR10[R] H,W 11111111 11111111		
000258_H	PCN11[R/W] B,H,W 00000000 000000-0		PCSR11[W] H,W XXXXXXXX XXXXXXXX		PPG11
$00025C_H$	PDUT11[W] H,W XXXXXXXX XXXXXXXX		PTMR11[R] H,W 11111111 11111111		
000260_H	PCN12[R/W] B,H,W 00000000 000000-0		PCSR12[W] H,W XXXXXXXX XXXXXXXX		PPG12
000264_H	PDUT12[W] H,W XXXXXXXX XXXXXXXX		PTMR12[R] H,W 11111111 11111111		
000268_H	PCN13[R/W] B,H,W 00000000 000000-0		PCSR13[W] H,W XXXXXXXX XXXXXXXX		PPG13
$00026C_H$	PDUT13[W] H,W XXXXXXXX XXXXXXXX		PTMR13[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000270_H	PCN14[R/W] B,H,W 00000000 000000-0		PCSR14[W] H,W XXXXXXXX XXXXXXXX		PPG14
000274_H	PDUT14[W] H,W XXXXXXXX XXXXXXXX		PTMR14[R] H,W 11111111 11111111		
000278_H	PCN15[R/W] B,H,W 00000000 000000-0		PCSR15[W] H,W XXXXXXXX XXXXXXXX		PPG15
$00027C_H$	PDUT15[W] H,W XXXXXXXX XXXXXXXX		PTMR15[R] H,W 11111111 11111111		
000280_H	PCN16[R/W] B,H,W 00000000 000000-0		PCSR16[W] H,W XXXXXXXX XXXXXXXX		PPG16
000284_H	PDUT16[W] H,W XXXXXXXX XXXXXXXX		PTMR16[R] H,W 11111111 11111111		
000288_H	PCN17[R/W] B,H,W 00000000 000000-0		PCSR17[W] H,W XXXXXXXX XXXXXXXX		PPG17
$00028C_H$	PDUT17[W] H,W XXXXXXXX XXXXXXXX		PTMR17[R] H,W 11111111 11111111		
000290_H	PCN18[R/W] B,H,W 00000000 000000-0		PCSR18[W] H,W XXXXXXXX XXXXXXXX		PPG18
000294_H	PDUT18[W] H,W XXXXXXXX XXXXXXXX		PTMR18[R] H,W 11111111 11111111		
000298_H	PCN19[R/W] B,H,W 00000000 000000-0		PCSR19[W] H,W XXXXXXXX XXXXXXXX		PPG19
$00029C_H$	PDUT19[W] H,W XXXXXXXX XXXXXXXX		PTMR19[R] H,W 11111111 11111111		
$0002A0_H$	PCN20[R/W] B,H,W 00000000 000000-0		PCSR20[W] H,W XXXXXXXX XXXXXXXX		PPG20
$0002A4_H$	PDUT20[W] H,W XXXXXXXX XXXXXXXX		PTMR20[R] H,W 11111111 11111111		
$0002A8_H$	PCN21[R/W] B,H,W 00000000 000000-0		PCSR21[W] H,W XXXXXXXX XXXXXXXX		PPG21
$0002AC_H$	PDUT21[W] H,W XXXXXXXX XXXXXXXX		PTMR21[R] H,W 11111111 11111111		
$0002B0_H$	PCN22[R/W] B,H,W 00000000 000000-0		PCSR22[W] H,W XXXXXXXX XXXXXXXX		PPG22
$0002B4_H$	PDUT22[W] H,W XXXXXXXX XXXXXXXX		PTMR22[R] H,W 11111111 11111111		
$0002B8_H$	PCN23[R/W] B,H,W 00000000 000000-0		PCSR23[W] H,W XXXXXXXX XXXXXXXX		PPG23
$0002BC_H$	PDUT23[W] H,W XXXXXXXX XXXXXXXX		PTMR23[R] H,W 11111111 11111111		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0002C0_H$	GTRS0[R/W] B,H,W -0000000 -0000000		GTRS1[R/W] B,H,W -0000000 -0000000		PPG Control
$0002C4_H$	GTRS2[R/W] B,H,W -0000000 -0000000		GTRS3[R/W] B,H,W -0000000 -0000000		
$0002C8_H$	GTRS4[R/W] B,H,W -0000000 -0000000		GTRS5[R/W] B,H,W -0000000 -0000000		
$0002CC_H$	GTRS6[R/W] B,H,W -0000000 -0000000		GTRS7[R/W] B,H,W -0000000 -0000000		
$0002D0_H$	GTRS8[R/W] B,H,W -0000000 -0000000		GTRS9[R/W] B,H,W -0000000 -0000000		
$0002D4_H$	GTRS10[R/W] B,H,W -0000000 -0000000		GTRS11[R/W] B,H,W -0000000 -0000000		
$0002D8_H$	GTREN0[R/W] H,W 00000000 00000000		GTREN1[R/W] H,W -------- 00000000		
$0002DC_H$	-		-		Reserved
$0002E0_H$	-	GATEC0[R/W] B,H,W ------00	-	GATEC2[R/W] B,H,W ------00	PPG GATE Control
$0002E4_H$	-	GATEC4[R/W] B,H,W ------00	-	GATEC8[R/W] B,H,W ------00	
$0002E8_H$	-	GATEC10[R/W] B,H,W ------00	-	GATEC12[R/W] B,H,W ------00	
$0002EC_H$	-	-	-	-	Reserved
$0002F0_H$	RCRH0[W] H,W 00000000	RCRL0[W] B,H,W 00000000	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	U/D counter 0
$0002F4_H$	CCR0[R/W] B,H 00000000 -0001000		-	CSR0[R] B 00000000	
$0002F8_H$	RCRH1[W] H,W 00000000	RCRL1[W] B,H,W 00000000	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	U/D counter 1
$0002FC_H$	CCR1[R/W] B,H 00000000 -0001000		-	CSR1[R] B 00000000	
000300_H	-				Reserved
000304_H	-	-	-	-	Reserved
000308_H	-				Reserved
$00030C_H$	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000310_H	-	-	MPUCR[R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	-	-	-	-	
000318_H	-				
$00031C_H$	-	-	-		
000320_H	DPVAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	-	-	DPVSR[R/W] H -------- 00000--0		
000328_H	DEAR[R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	-	-	DESR[R/W] H -------- 00000--0		
000330_H	PABR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	-	-	PACR0[R/W] H 000000-0 00000--0		
000338_H	PABR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	-	-	PACR1[R/W] H 000000-0 00000--0		
000340_H	PABR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	-	-	PACR2[R/W] H 000000-0 00000--0		
000348_H	PABR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	-	-	PACR3[R/W] H 000000-0 00000--0		
000350_H	PABR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000354_H	-	-	PACR4[R/W] H 000000-0 00000--0		
000358_H	PABR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	-	-	PACR5[R/W] H 000000-0 00000--0		
000360_H	PABR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	-	-	PACR6[R/W] H 000000-0 00000--0		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000368_H	PABR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
$00036C_H$	-	-	PACR7[R/W] H 000000-0 00000--0		
000370_H	-				Reserved [S]
000374_H	-	-	-		
000378_H	-				
$00037C_H$	-	-	-		
000380_H	-				
000384_H	-	-	-		
000388_H	-				
$00038C_H$	-	-	-		
000390_H	-				
000394_H	-	-	-		Reserved [S]
000398_H	-				
$00039C_H$	-	-	-		
$0003A0_H$	-				
$0003A4_H$	-	-	-		
$0003A8_H$	-				
$0003AC_H$	-	-	-		
$0003B0_H$ | $0003FC_H$	-	-	-	-	Reserved [S]
000400_H	ICSEL0[R/W] B,H,W -----000	ICSEL1[R/W] B,H,W -------0	ICSEL2[R/W] B,H,W -------0	ICSEL3[R/W] B,H,W -------0	Generation and clearing of DMA transfer requests
000404_H	ICSEL4[R/W] B,H,W -------0	ICSEL5[R/W] B,H,W -------0	ICSEL6[R/W] B,H,W -------0	ICSEL7[R/W] B,H,W -----000	
000408_H	ICSEL8[R/W] B,H,W -------0	ICSEL9[R/W] B,H,W -------0	ICSEL10[R/W] B,H,W -----000	ICSEL11[R/W] B,H,W -----000	
$00040C_H$	ICSEL12[R/W] B,H,W -----000	ICSEL13[R/W] B,H,W -----000	ICSEL14[R/W] B,H,W -----000	ICSEL15[R/W] B,H,W -------0	
000410_H	ICSEL16[R/W] B,H,W -------0	ICSEL17[R/W] B,H,W -------0	ICSEL18[R/W] B,H,W -------0	ICSEL19[R/W] B,H,W -------0	
000414_H	ICSEL20[R/W] B,H,W -------0	ICSEL21[R/W] B,H,W -----000	ICSEL22[R/W] B,H,W -----000	ICSEL23[R/W] B,H,W -----000	
000418_H	ICSEL24[R/W] B,H,W -----000	ICSEL25[R/W] B,H,W -----000	ICSEL26[R/W] B,H,W -------0	ICSEL27[R/W] B,H,W -------0	
$00041C_H$	-	-	-	-	
000420_H	-	-	-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000424_H | $00043C_H$	-	-	-	-	Reserved
000440_H	ICR00[R/W] B,H,W ---11111	ICR01[R/W] B,H,W ---11111	ICR02[R/W] B,H,W ---11111	ICR03[R/W] B,H,W ---11111	Interrupt controller [S]
000444_H	ICR04[R/W] B,H,W ---11111	ICR05[R/W] B,H,W ---11111	ICR06[R/W] B,H,W ---11111	ICR07[R/W] B,H,W ---11111	
000448_H	ICR08[R/W] B,H,W ---11111	ICR09[R/W] B,H,W ---11111	ICR10[R/W] B,H,W ---11111	ICR11[R/W] B,H,W ---11111	
$00044C_H$	ICR12[R/W] B,H,W ---11111	ICR13[R/W] B,H,W ---11111	ICR14[R/W] B,H,W ---11111	ICR15[R/W] B,H,W ---11111	
000450_H	ICR16[R/W] B,H,W ---11111	ICR17[R/W] B,H,W ---11111	ICR18[R/W] B,H,W ---11111	ICR19[R/W] B,H,W ---11111	
000454_H	ICR20[R/W] B,H,W ---11111	ICR21[R/W] B,H,W ---11111	ICR22[R/W] B,H,W ---11111	ICR23[R/W] B,H,W ---11111	
000458_H	ICR24[R/W] B,H,W ---11111	ICR25[R/W] B,H,W ---11111	ICR26[R/W] B,H,W ---11111	ICR27[R/W] B,H,W ---11111	
$00045C_H$	ICR28[R/W] B,H,W ---11111	ICR29[R/W] B,H,W ---11111	ICR30[R/W] B,H,W ---11111	ICR31[R/W] B,H,W ---11111	
000460_H	ICR32[R/W] B,H,W ---11111	ICR33[R/W] B,H,W ---11111	ICR34[R/W] B,H,W ---11111	ICR35[R/W] B,H,W ---11111	
000464_H	ICR36[R/W] B,H,W ---11111	ICR37[R/W] B,H,W ---11111	ICR38[R/W] B,H,W ---11111	ICR39[R/W] B,H,W ---11111	
000468_H	ICR40[R/W] B,H,W ---11111	ICR41[R/W] B,H,W ---11111	ICR42[R/W] B,H,W ---11111	ICR43[R/W] B,H,W ---11111	
$00046C_H$	ICR44[R/W] B,H,W ---11111	ICR45[R/W] B,H,W ---11111	ICR46[R/W] B,H,W ---11111	ICR47[R/W] B,H,W ---11111	
000470_H | $00047C_H$	-	-	-	-	Reserved [S]
000480_H	RSTRR[R] B,H,W XXXX--XX	RSTCR[R/W] B,H,W 111----0	STBCR[R/W] B,H,W* 000---11	-	Reset control [S] Power consumption control [S] * Writing to STBCR by DMA is disabled.
000484_H	-	-	-	-	Reserved [S]
000488_H	DIVR0[R/W] B,H,W 000-----	DIVR1[R/W] B,H,W 0001----	DIVR2[R/W] B,H,W 0011----	-	Clock control [S]
$00048C_H$	-	-	-	-	Reserved [S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000490_H	IORR0[R/W] B,H,W -0000000	IORR1[R/W] B,H,W -0000000	IORR2[R/W] B,H,W -0000000	IORR3[R/W] B,H,W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B,H,W -0000000	IORR5[R/W] B,H,W -0000000	IORR6[R/W] B,H,W -0000000	IORR7[R/W] B,H,W -0000000	
000498_H	-	-	-	-	
$00049C_H$	-	-	-	-	
$0004A0_H$	-	-	-	-	Reserved
$0004A4_H$	CANPRE[R/W] B,H,W ----0000	-	-	-	CAN prescaler
$0004A8_H$ | $0004AC_H$	-	-	-	-	Reserved
$0004B0_H$	-	-	-	-	Reserved
$0004B4_H$ | $0004C0_H$	-	-	-	-	Reserved
$0004C4_H$	CUCR1[R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		WDT1 calibration
$0004C8_H$	CUTR1[R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$ | $0004DC_H$	-	-	-	-	Reserved
$0004E0_H$	-	-	CSCFG[R/W] B,H,W ---0----	CMCFG[R/W] B,H,W 00000000	Clock monitor
$0004E4_H$	-	-	-	-	
$0004E8_H$	PLL2DIVM[R/W] B,H,W ----0000	PLL2DIVN[R/W] B,H,W -0000000	PLL2DIVG[R/W] B,H,W ----0000	PLL2MULG[R/W] B,H,W 00000000	FlexRay clock control
$0004EC_H$	PLL2CTRL[R/W] B,H,W ----0000	PLL2DIVK[R/W] B,H,W -------0	CLKR2[R/W] B,H,W 000--000	-	
$0004F0_H$ | $0004FC_H$	-	-	-	-	Reserved
000500_H	-				Reserved
000504_H	-				Reserved
000508_H | $00050C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000510_H	CSELR[R/W] B,H,W -0----00	CMONR[R] B,H,W -01---00	MTMCR[R/W] B,H,W 00001111	-	Clock control [S]
000514_H	PLLCR[R/W] B,H,W 00-00000 11110000		CSTBR[R/W] B,H,W ----0000	PTMCR[R/W] B,H,W 00------	
000518_H	-	-	CPUAR[R/W] B,H,W 0---XXXX	-	Reset [S]
$00051C_H$	-	-	-	-	Reserved [S]
000520_H	CCPSSELR[R/W] B,H,W -------0	-	-	CCPSDIVR[R/W] B,H,W -000-000	Clock control 2
000524_H	-	CCPLLFBR[R/W] B,H,W -0000000	CCSSFBR0[R/W] B,H,W --000000	CCSSFBR1[R/W] B,H,W ---00000	
000528_H	-	CCSSCCR0[R/W] B,H,W ----0000	CCSSCCR1[R/W] H,W 000----- --------		
$00052C_H$	-	CCCGRCR0[R/W] B,H,W 00----00	CCCGRCR1[R/W] B,H,W 00000000	CCCGRCR2[R/W] B,H,W 00000000	
000530_H	-	-	CCPMUCR0[R/W] B,H,W 0-----00	CCPMUCR1[R/W] B,H,W 0--00000	
000534_H	-	-	-	-	
000538_H	-	-	-	-	
$00053C_H$	-	-	-	-	
000540_H | $00054C_H$	-	-	-	-	Reserved
000550_H	EIRR0[R/W] B,H,W XXXXXXXX	ENIR0[R/W] B,H,W 00000000	ELVR0[R/W] B,H,W 00000000 00000000		External interrupt (INT0 to 7)
000554_H | 000568_H	-	-	-	-	Reserved
$00056C_H$	-	CSVCR[R/W] B -0--1--0	-	-	CSV
000570_H	CRTR[R/W] B,H,W 01111111	-	-	-	WDT1 calibration (trimming)
000574_H | $00057C_H$	-	-	-	-	Reserved
000580_H	REGSEL[R/W] B,H,W 01--110-	-	-	-	Regulator control

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000584_H	LVD5R[R/W] B,H,W -------1	LVD5F[R/W] B,H,W 0-010--1	LVD[R/W] B,H,W 01000--0	-	Low-voltage detection
000588_H | $00058C_H$	-	-	-	-	Reserved
000590_H	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR[R/W] B,H,W 0-00----	PWRTMCTL[R/W] B,H,W -----011	-	PMU
000594_H	-	PMUINTF1[R/W] B,H,W 00000000	PMUINTF2[R/W] B,H,W -00-----	-	
000598_H	-	-	-	-	
$00059C_H$	-	-	-	-	
$0005A0_H$ | $0005FC_H$	-	-	-	-	Reserved
000600_H	ASR0[R/W] W 00000000 00000000 -------- 1111-001				External bus interface [S]
000604_H	ASR1[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000608_H	ASR2[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
$00060C_H$	ASR3[R/W] W XXXXXXXX XXXXXXXX -------- XXXX-XX0				
000610_H | $00063C_H$	-	-	-	-	Reserved[S]
000640_H	ACR0[R/W] W -------- -------- -------- 00--00--				External bus interface [S]
000644_H	ACR1[R/W] W -------- -------- -------- XX--XX--				
000648_H	ACR2[R/W] W -------- -------- -------- XX--XX--				
$00064C_H$	ACR3[R/W] W -------- -------- -------- XX--XX--				
000650_H | $00067C_H$	-	-	-	-	Reserved[S]

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000680_H	AWR0[R/W] W ----1111 00000000 11110000 00000-0-				External bus interface [S]
000684_H	AWR1[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000688_H	AWR2[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
$00068C_H$	AWR3[R/W] W ----XXXX XXXXXXXX XXXXXXXX XXXXX-X-				
000690_H | $0006BC_H$	-	-	-	-	Reserved[S]
$0006C0_H$	DMAR0[R/W] W -------- -------- -------- ----0000				External bus interface [S]
$0006C4_H$	DMAR1[R/W] W -------- -------- -------- ----0000				
$0006C8_H$	DMAR2[R/W] W -------- -------- -------- ----0000				
$0006CC_H$	DMAR3[R/W] W -------- -------- -------- ----0000				
$0006D0_H$ | $0006F0_H$	-	-	-	-	Reserved
$0006F4_H$	-				Reserved
$0006F8_H$ | $0006FC_H$	-	-	-	-	Reserved
000700_H	-				Reserved
000704_H | $00070C_H$	-	-	-	-	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	-	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720_H | $0007F8_H$	-	-	-	-	Reserved
$0007FC_H$	BMODR[R] B,H,W XXXXXXXX	-	-	-	Operation mode

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
000800_H | $00083C_H$	-	-	-	-	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		-	FSTR[R/W] B -----001	Flash memory register [S]
000844_H	-	-	-	-	Reserved [S]
000848_H | 000854_H	-	-	-	-	Reserved [S]
000858_H	-	-	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ | $00087C_H$	-	-	-	-	Reserved [S]
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008A4_H$	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0008B8_H$	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
$0008BC_H$	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008F4_H$	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F8_H$	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008FC_H$	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900_H | $000BF8_H$	-	-	-	-	Reserved
$000BFC_H$	-	-	UER[W] B,H,W -------- -------X		OCDU

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C00_H$	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
$000C04_H$	DCSR0[R/W] H 0------- -----000		DTCR0[R/W] H 00000000 00000000		
$000C08_H$	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1[R/W] H 0------- -----000		DTCR1[R/W] H 00000000 00000000		
$000C18_H$	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2[R/W] H 0------- -----000		DTCR2[R/W] H 00000000 00000000		
$000C28_H$	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
$000C38_H$	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		
$000C48_H$	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C4C_H$	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		DMA controller [S]
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$ | $000DF0_H$	-	-	-	-	
$000DF4_H$	-	-	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	-	-	-	-	Reserved [S]
$000E00_H$	DDR00[R/W] B,H 00000000	DDR01[R/W] B,H 00000000	DDR02[R/W] B,H 00000000	DDR03[R/W] B,H 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H 00000000	DDR05[R/W] B,H 00000000	DDR06[R/W] B,H 00000000	DDR07[R/W] B,H 00000000	
$000E08_H$	DDR08[R/W] B,H 00000000	DDR09[R/W] B,H 00000000	DDR10[R/W] B,H 00000000	DDR11[R/W] B,H 00000000	
$000E0C_H$	DDR12[R/W] B,H 00000000	DDR13[R/W] B,H 00-00000	-	-	
$000E10_H$ | $000E1C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E20_H$	PFR00[R/W] B,H 00000000	PFR01[R/W] B,H 00000000	PFR02[R/W] B,H 00000000	PFR03[R/W] B,H 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H 00000000	PFR05[R/W] B,H 00000000	PFR06[R/W] B,H 00000000	PFR07[R/W] B,H 00000000	
$000E28_H$	PFR08[R/W] B,H 00000000	PFR09[R/W] B,H 00000000	PFR10[R/W] B,H 00000000	PFR11[R/W] B,H 00000000	
$000E2C_H$	PFR12[R/W] B,H 00000000	PFR13[R/W] B,H 00-00000	-	-	
$000E30_H$ | $000E3C_H$	-	-	-	-	Reserved
$000E40_H$	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
$000E44_H$	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W XXXXXXXX	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
$000E48_H$	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
$000E4C_H$	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	-	-	
$000E50_H$ | $000E5C_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000E60_H$	EPFR00[R/W] B,H -----000	EPFR01[R/W] B,H ------00	EPFR02[R/W] B,H --000000	EPFR03[R/W] B,H 00000000	Extended port function register
$000E64_H$	EPFR04[R/W] B,H 00000000	EPFR05[R/W] B,H 00000000	EPFR06[R/W] B,H ------00	EPFR07[R/W] B,H ----0000	
$000E68_H$	EPFR08[R/W] B,H ----0000	EPFR09[R/W] B,H -------0	EPFR10[R/W] B,H 00000000	EPFR11[R/W] B,H ----0000	
$000E6C_H$	-	EPFR13[R/W] B,H -------1	EPFR14[R/W] B,H -0000000	EPFR15[R/W] B,H -0000000	
$000E70_H$	EPFR16[R/W] B,H --000000	EPFR17[R/W] B,H 00000000	EPFR18[R/W] B,H 00000000	EPFR19[R/W] B,H 00000000	
$000E74_H$	EPFR20[R/W] B,H 00000000	EPFR21[R/W] B,H 00000000	EPFR22[R/W] B,H 00000000	EPFR23[R/W] B,H 00000000	
$000E78_H$	EPFR24[R/W] B,H 00000000	EPFR25[R/W] B,H 00000000	EPFR26[R/W] B,H 00000000	EPFR27[R/W] B,H 00000000	
$000E7C_H$	EPFR28[R/W] B,H 00000000	EPFR29[R/W] B,H 00000000	EPFR30[R/W] B,H 00000000	EPFR31[R/W] B,H 00000000	
$000E80_H$	EPFR32[R/W] B,H 00000000	-	-	-	
$000E84_H$ | $000EBC_H$	-	-	-	-	Reserved
$000EC0_H$	PPER00[R/W] B,H 00000000	PPER01[R/W] B,H 00000000	PPER02[R/W] B,H 00000000	PPER03[R/W] B,H 00000000	Port pull-up/down enable register
$000EC4_H$	PPER04[R/W] B,H 00000000	PPER05[R/W] B,H 00000000	PPER06[R/W] B,H 00000000	PPER07[R/W] B,H 00000000	
$000EC8_H$	PPER08[R/W] B,H 00000000	PPER09[R/W] B,H 00000000	PPER10[R/W] B,H 00000000	PPER11[R/W] B,H 00000000	
$000ECC_H$	PPER12[R/W] B,H 00000000	PPER13[R/W] B,H 00-00000	-	-	
$000ED0_H$ | $000EDC_H$	-	-	-	-	Reserved
$000EE0_H$	PILR00[R/W] B,H 11111111	PILR01[R/W] B,H 11111111	PILR02[R/W] B,H 11111111	PILR03[R/W] B,H 11111111	Port input level selection register
$000EE4_H$	PILR04[R/W] B,H 11111111	PILR05[R/W] B,H 11111111	PILR06[R/W] B,H 11111111	PILR07[R/W] B,H 11111111	
$000EE8_H$	PILR08[R/W] B,H 11111111	PILR09[R/W] B,H 11111111	PILR10[R/W] B,H 11111111	PILR11[R/W] B,H 11111111	
$000EEC_H$	PILR12[R/W] B,H 11111111	PILR13[R/W] B,H 11-11111	-	-	
$000EF0_H$ | $000EFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$000F00_H$ | $000F1C_H$	-	-	-	-	Reserved
$000F20_H$	PODR00[R/W] B,H 00000000	PODR01[R/W] B,H 00000000	PODR02[R/W] B,H 00000000	PODR03[R/W] B,H 00000000	Port output drive register
$000F24_H$	PODR04[R/W] B,H 00000000	PODR05[R/W] B,H 00000000	PODR06[R/W] B,H 00000000	PODR07[R/W] B,H 00000000	
$000F28_H$	PODR08[R/W] B,H 00000000	PODR09[R/W] B,H 00000000	PODR10[R/W] B,H 00000000	PODR11[R/W] B,H 00000000	
$000F2C_H$	PODR12[R/W] B,H 00000000	PODR13[R/W] B,H 00-00000	-	-	
$000F30_H$ | $000F3C_H$	-	-	-	-	Reserved
$000F40_H$	PORTEN[R/W] B,H,W ------00	-	-	-	Port input enable register
$000F44_H$	KEYCDR[R/W] H 00000000 00000000		-	-	Port key code
$000F48_H$	ADERH[R/W] B,H -------- 11111111		ADERL[R/W] B,H 11111111 11111111		Analog input enable register
$000F4C_H$	DAER[R/W] B,H -------0	-	-	-	Analog output enable register
$000F50_H$ | $000FFC_H$	-	-	-	-	Reserved
001000_H	SACR[R/W] B,H,W -------0	PICD[R/W] B,H,W ----0011	-	-	Synchronous/asynchronous switch control
001004_H | $0010BC_H$	-	-	-	-	Reserved
$0010C0_H$	-	-	-	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation
$0010C4_H$	CRCINIT[R/W] B,H,W 11111111 11111111 11111111 11111111				
$0010C8_H$	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
$0010CC_H$	CRCR[R] B,H,W 11111111 11111111 11111111 11111111				
$0010D0_H$ | $0010FC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001100_H	TCGS[R/W] B,H,W ------00	-	-	TCGSE[R/W] B,H,W --000000	Free-run timer simultaneous activation
001104_H	CPCLRB0/CPCLR0[R/W] H,W 11111111 11111111		TCDT0[R/W] H,W 00000000 00000000		Free-run timer 0
001108_H	TCCS0[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00110C_H$	CPCLRB1/CPCLR1[R/W] H,W 11111111 11111111		TCDT1[R/W] H,W 00000000 00000000		Free-run timer 1
001110_H	TCCS1[R/W] B,H,W 00000000 01000000 ----0000 --------				
001114_H	CPCLRB2/CPCLR2[R/W] H,W 11111111 11111111		TCDT2[R/W] H,W 00000000 00000000		Free-run timer 2
001118_H	TCCS2[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00111C_H$	CPCLRB3/CPCLR3[R/W] H,W 11111111 11111111		TCDT3[R/W] H,W 00000000 00000000		Free-run timer 3
001120_H	TCCS3[R/W] B,H,W 00000000 01000000 ----0000 --------				
001124_H	CPCLRB4/CPCLR4[R/W] H,W 11111111 11111111		TCDT4[R/W] H,W 00000000 00000000		Free-run timer 4
001128_H	TCCS4[R/W] B,H,W 00000000 01000000 ----0000 --------				
$00112C_H$	CPCLRB5/CPCLR5[R/W] H,W 11111111 11111111		TCDT5[R/W] H,W 00000000 00000000		Free-run timer 5
001130_H	TCCS5[R/W] B,H,W 00000000 01000000 ----0000 --------				
001134_H	FRS0[R/W] B,H,W -------- -000-000 -000-000 -000-000				Free-run timer selection
001138_H	FRS1[R/W] B,H,W -------- -------- -000-000 -000-000				
$00113C_H$	FRS2[R/W] B,H,W -------- -000-000 -000-000 -000-000				
001140_H	FRS3[R/W] B,H,W -------- -------- -000-000 -000-000				
001144_H	FRS4[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001148_H	FRS5[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
$00114C_H$	FRS6[R/W] B,H,W -000-000 -000-000 -000-000 -000-000				
001150_H	-				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001154_H	OCCPB0/OCCP0[R/W] H,W 00000000 00000000		OCCPB1/OCCP1[R/W] H,W 00000000 00000000		Output compare 0/1
001158_H	OCS01[R/W] B,H,W -110--00 00001100		-	OCMOD01[R/W] B,H,W ------00	
$00115C_H$	OCCPB2/OCCP2[R/W] H,W 00000000 00000000		OCCPB3/OCCP3[R/W] H,W 00000000 00000000		Output compare 2/3
001160_H	OCS23[R/W] B,H,W -110--00 00001100		-	OCMOD23[R/W] B,H,W ------00	
001164_H	OCCPB4/OCCP4[R/W] H,W 00000000 00000000		OCCPB5/OCCP5[R/W] H,W 00000000 00000000		Output compare 4/5
001168_H	OCS45[R/W] B,H,W -110--00 00001100		-	OCMOD45[R/W] B,H,W ------00	
$00116C_H$	OCCPB6/OCCP6[R/W] H,W 00000000 00000000		OCCPB7/OCCP7[R/W] H,W 00000000 00000000		Output compare 6/7
001170_H	OCS67[R/W] B,H,W -110--00 00001100		-	OCMOD67[R/W] B,H,W ------00	
001174_H	OCCPB8/OCCP8[R/W] H,W 00000000 00000000		OCCPB9/OCCP9[R/W] H,W 00000000 00000000		Output compare 8/9
001178_H	OCS89[R/W] B,H,W -110--00 00001100		-	OCMOD89[R/W] B,H,W ------00	
$00117C_H$	OCCPB10/OCCP10[R/W] H,W 00000000 00000000		OCCPB11/OCCP11[R/W] H,W 00000000 00000000		Output compare 10/11
001180_H	OCS1011[R/W] B,H,W -110--00 00001100		-	OCMOD1011 [R/W] B,H,W ------00	
001184_H	IPCP0[R] H,W 00000000 00000000		IPCP1[R] H,W 00000000 00000000		Input capture 0/1
001188_H	ICS01[R/W] B,H,W ------00 00000000		-	LSYNS[R/W] B,H,W ---00000	
$00118C_H$	IPCP2[R] H,W 00000000 00000000		IPCP3[R] H,W 00000000 00000000		Input capture 2/3
001190_H	ICS23[R/W] B,H,W ------00 00000000		-	-	
001194_H	IPCP4[R] H,W 00000000 00000000		IPCP5[R] H,W 00000000 00000000		Input capture 4/5
001198_H	ICS45[R/W] B,H,W ------00 00000000		-	-	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00119C$_H$	IPCP6[R] H,W 00000000 00000000		IPCP7[R] H,W 00000000 00000000		Input capture 6/7
0011A0$_H$	ICS67[R/W] B,H,W ------00 00000000		-	-	
0011A4$_H$	DTSR[R/W] B,H,W ------10	-	-	-	DTTI selection
0011A8$_H$	TMRR0[R/W] H,W 00000000 00000001		TMRR1[R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0011AC$_H$	TMRR2[R/W] H,W 00000000 00000001		-	-	
0011B0$_H$	DTSCR0[R/W] B,H,W 00000000	DTSCR1[R/W] B,H,W 00000000	DTSCR2[R/W] B,H,W 00000000	-	
0011B4$_H$	-	DTIR0[R/W] B,H,W 000000--	-	DTMNS0[R/W] B,H,W 00---000	
0011B8$_H$	-	SIGCR10[R/W] B,H,W 00000000	-	SIGCR20[R/W] B,H,W 000000-1	
0011BC$_H$	PICS0[R/W] B,H,W 000000-- -------- -------- --------				
0011C0$_H$	TMRR3[R/W] H,W 00000000 00000001		TMRR4[R/W] H,W 00000000 00000001		Waveform generator 3/4/5
0011C4$_H$	TMRR5[R/W] H,W 00000000 00000001		-	-	
0011C8$_H$	DTSCR3[R/W] B,H,W 00000000	DTSCR4[R/W] B,H,W 00000000	DTSCR5[R/W] B,H,W 00000000	-	
0011CC$_H$	-	DTIR1[R/W] B,H,W 000000--	-	DTMNS1[R/W] B,H,W 00---000	
0011D0$_H$	-	SIGCR11[R/W] B,H,W 00000000	-	SIGCR21[R/W] B,H,W 000000-1	
0011D4$_H$	PICS1[R/W] B,H,W 000000-- -------- -------- --------				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0011D8$_H$	-	-	-	-	12-bit A/D converter
0011DC$_H$	ADTSS[R/W] B,H,W -------0	-	-	-	
0011E0$_H$	ADTSE[R/W] B,H,W -------- 00000000 00000000 00000000				
0011E4$_H$	ADCOMP0/ADCOMPB0[R/W] H,W 00000000 00000000		ADCOMP1/ADCOMPB1[R/W] H,W 00000000 00000000		
0011E8$_H$	ADCOMP2/ADCOMPB2[R/W] H,W 00000000 00000000		ADCOMP3/ADCOMPB3[R/W] H,W 00000000 00000000		
0011EC$_H$	ADCOMP4/ADCOMPB4[R/W] H,W 00000000 00000000		ADCOMP5/ADCOMPB5[R/W] H,W 00000000 00000000		
0011F0$_H$	ADCOMP6/ADCOMPB6[R/W] H,W 00000000 00000000		ADCOMP7/ADCOMPB7[R/W] H,W 00000000 00000000		
0011F4$_H$	ADCOMP8/ADCOMPB8[R/W] H,W 00000000 00000000		ADCOMP9/ADCOMPB9[R/W] H,W 00000000 00000000		
0011F8$_H$	ADCOMP10/ADCOMPB10[R/W] H,W 00000000 00000000		ADCOMP11/ADCOMPB11[R/W] H,W 00000000 00000000		
0011FC$_H$	ADCOMP12/ADCOMPB12[R/W] H,W 00000000 00000000		ADCOMP13/ADCOMPB13[R/W] H,W 00000000 00000000		
001200$_H$	ADCOMP14/ADCOMPB14[R/W] H,W 00000000 00000000		ADCOMP15/ADCOMPB15[R/W] H,W 00000000 00000000		
001204$_H$	ADCOMP16/ADCOMPB16[R/W] H,W 00000000 00000000		ADCOMP17/ADCOMPB17[R/W] H,W 00000000 00000000		
001208$_H$	ADCOMP18/ADCOMPB18[R/W] H,W 00000000 00000000		ADCOMP19/ADCOMPB19[R/W] H,W 00000000 00000000		
00120C$_H$	ADCOMP20/ADCOMPB20[R/W] H,W 00000000 00000000		ADCOMP21/ADCOMPB21[R/W] H,W 00000000 00000000		
001210$_H$	ADCOMP22/ADCOMPB22[R/W] H,W 00000000 00000000		ADCOMP23/ADCOMPB23[R/W] H,W 00000000 00000000		
001214$_H$	-	-	-	-	
001218$_H$	-	-	-	-	
00121C$_H$	-	-	-	-	
001220$_H$	-	-	-	-	
001224$_H$	ADTCS0[R/W] B,H,W 00000000 0010-000		ADTCS1[R/W] B,H,W 00000000 0010-000		
001228$_H$	ADTCS2[R/W] B,H,W 00000000 0010-000		ADTCS3[R/W] B,H,W 00000000 0010-000		
00122C$_H$	ADTCS4[R/W] B,H,W 00000000 0010-000		ADTCS5[R/W] B,H,W 00000000 0010-000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001230_H	ADTCS6[R/W] B,H,W 00000000 0010-000		ADTCS7[R/W] B,H,W 00000000 0010-000		12-bit A/D converter
001234_H	ADTCS8[R/W] B,H,W 00000000 0010-000		ADTCS9[R/W] B,H,W 00000000 0010-000		
001238_H	ADTCS10[R/W] B,H,W 00000000 0010-000		ADTCS11[R/W] B,H,W 00000000 0010-000		
$00123C_H$	ADTCS12[R/W] B,H,W 00000000 0010-000		ADTCS13[R/W] B,H,W 00000000 0010-000		
001240_H	ADTCS14[R/W] B,H,W 00000000 0010-000		ADTCS15[R/W] B,H,W 00000000 0010-000		
001244_H	ADTCS16[R/W] B,H,W 00000000 00100000		ADTCS17[R/W] B,H,W 00000000 00100000		
001248_H	ADTCS18[R/W] B,H,W 00000000 00100000		ADTCS19[R/W] B,H,W 00000000 00100000		
$00124C_H$	ADTCS20[R/W] B,H,W 00000000 00100000		ADTCS21[R/W] B,H,W 00000000 00100000		
001250_H	ADTCS22[R/W] B,H,W 00000000 00100000		ADTCS23[R/W] B,H,W 00000000 00100000		
001254_H	-	-	-	-	
001258_H	-	-	-	-	
$00125C_H$	-	-	-	-	
001260_H	-	-	-	-	
001264_H	ADTCD0[R] B,H,W 10--0000 00000000		ADTCD1[R] B,H,W 10--0000 00000000		
001268_H	ADTCD2[R] B,H,W 10--0000 00000000		ADTCD3[R] B,H,W 10--0000 00000000		
$00126C_H$	ADTCD4[R] B,H,W 10--0000 00000000		ADTCD5[R] B,H,W 10--0000 00000000		
001270_H	ADTCD6[R] B,H,W 10--0000 00000000		ADTCD7[R] B,H,W 10--0000 00000000		
001274_H	ADTCD8[R] B,H,W 10--0000 00000000		ADTCD9[R] B,H,W 10--0000 00000000		
001278_H	ADTCD10[R] B,H,W 10--0000 00000000		ADTCD11[R] B,H,W 10--0000 00000000		
$00127C_H$	ADTCD12[R] B,H,W 10--0000 00000000		ADTCD13[R] B,H,W 10--0000 00000000		
001280_H	ADTCD14[R] B,H,W 10--0000 00000000		ADTCD15[R] B,H,W 10--0000 00000000		
001284_H	ADTCD16[R] B,H,W 10--0000 00000000		ADTCD17[R] B,H,W 10--0000 00000000		
001288_H	ADTCD18[R] B,H,W 10--0000 00000000		ADTCD19[R] B,H,W 10--0000 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
00128C$_H$	ADTCD20[R] B,H,W 10--0000 00000000		ADTCD21[R] B,H,W 10--0000 00000000		12-bit A/D converter
001290$_H$	ADTCD22[R] B,H,W 10--0000 00000000		ADTCD23[R] B,H,W 10--0000 00000000		
001294$_H$	-	-	-	-	
001298$_H$	-	-	-	-	
00129C$_H$	-	-	-	-	
0012A0$_H$	-	-	-	-	
0012A4$_H$	ADCS0[R/W] B,H,W 0------- --------		ADCH0[R] B,H,W -----000	ADMD0[R/W] B,H,W ----0000	
0012A8$_H$	ADCS1[R/W] B,H,W 0------- --------		ADCH1[R] B,H,W -----000	ADMD1[R/W] B,H,W ----0000	
0012AC$_H$	ADCS2[R/W] B,H,W 0------- --------		ADCH2[R] B,H,W -----000	ADMD2[R/W] B,H,W ----0000	
0012B0$_H$ | 0012FC$_H$	-	-	-	-	Reserved
001300$_H$	-	-	-	-	Reserved
001304$_H$	-	-	-	-	
001308$_H$	-	-	-	-	
00130C$_H$	-	-	-	-	
001310$_H$	-	-	-	-	
001314$_H$	-	-	-	-	
001318 $_H$	-	-	-	-	
00131C$_H$	-	-	-	-	
001320$_H$	-	-	-	-	
001324$_H$	-		-		
001328$_H$	-	-	-	-	
00132C$_H$	-	-	-	-	
001330$_H$	-		-		
001334$_H$ | 0013FC$_H$	-	-	-	-	Reserved
001400$_H$	DACR[R/W] B,H,W -------0	-	DADR[R/W] H,W ------XX XXXXXXXX		DAC
001404$_H$ | 0014FC$_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001500_H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000000-0	SSR0 [R/W] B,H,W 0--00011	ESCR0/(IBSR0) [R/W] B,H,W 00000000	Multi Function Serial I/F 0 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001504_H	-/(RDR10/(TDR10))[R/W] H,W -------- -------- *3		RDR00/(TDR00)[R/W] B,H,W -------0 00000000 *1		
001508_H	SACSR0[R/W] B,H,W 0----000 00000000		STMR0[R] B,H,W 00000000 00000000		
$00150C_H$	STMCR0[R/W] B,H,W 00000000 00000000		-/(SFUR0) [R/W] B,H,W -------- -------- *4		
001510_H	-	-	-/(SFLR10) [R/W] B,H,W -------- *4	-/(SFLR00) [R/W] B,H,W -------- *4	
001514_H	-	-	-	-	
001518_H	-	-	-	-	
$00151C_H$	BGR0[R/W] H,W 00000000 00000000		-/(ISMK0)[R/W] B,H,W -------- *2	-/(ISBA0)[R/W] B,H,W -------- *2	
001520_H	FCR10[R/W] B,H,W 00-00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	
001524_H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1[R/W] B,H,W 000000-0	SSR1[R/W] B,H,W 0--00011	ESCR1/(IBSR1) [R/W] B,H,W 00000000	Multi Function Serial I/F 1 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001528_H	-/(RDR11/(TDR11))[R/W] H,W -------- -------- *3		RDR01/(TDR01)[R/W] B,H,W -------0 00000000 *1		
$00152C_H$	SACSR1[R/W] B,H,W 0----000 00000000		STMR1[R] B,H,W 00000000 00000000		
001530_H	STMCR1[R/W] B,H,W 00000000 00000000		-/(SCSCR1/SFUR1) [R/W] B,H,W -------- -------- *3,*4		
001534_H	-/(SCSTR31) [R/W] B,H,W -------- *3	-/(SCSTR21) [R/W] B,H,W -------- *3	-/(SCSTR11/SFLR11) [R/W] B,H,W -------- *3,*4	-/(SCSTR01/SFLR01) [R/W] B,H,W -------- *3,*4	
001538_H	-	-	-	-	
$00153C_H$	-	-	-	TBYTE01[R/W] B,H,W 00000000	
001540_H	BGR1[R/W] H,W 00000000 00000000		-/(ISMK1)[R/W] B,H,W -------- *2	-/(ISBA1)[R/W] B,H,W -------- *2	
001544_H	FCR11[R/W] B,H,W 00-00100	FCR01[R/W] B,H,W -0000000	FBYTE21[R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001548$_H$	SCR2[R/W] B,H,W 0--00000	SMR2[R/W] B,H,W 000000-0	SSR2[R/W] B,H,W 0--00011	ESCR2[R/W] B,H,W 00000000	Multi Function Serial I/F 2 *1: Byte access is possible only for access to lower 8 bits. *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
00154C$_H$	-/(RDR12/(TDR12))[R/W] H,W -------- -------- *3		RDR02/(TDR02)[R/W] B,H,W -------0 00000000 *1		
001550$_H$	SACSR2[R/W] B,H,W 0----000 00000000		STMR2[R] B,H,W 00000000 00000000		
001554$_H$	STMCR2[R/W] B,H,W 00000000 00000000		-/(SCSCR2/SFUR2) [R/W] B,H,W -------- -------- *3,*4		
001558$_H$	-/(SCSTR32) [R/W] B,H,W -------- *3	-/(SCSTR22) [R/W] B,H,W -------- *3	-/(SCSTR12/SFLR12) [R/W] B,H,W -------- *3,*4	-/(SCSTR02/SFLR02) [R/W] B,H,W -------- *3,*4	
00155C$_H$	-	-	-	-	
001560$_H$	-	-	-	TBYTE02[R/W] B,H,W 00000000	
001564$_H$	BGR2[R/W] H,W 00000000 00000000		-	-	
001568$_H$	FCR12[R/W] B,H,W 00-00100	FCR02[R/W] B,H,W -0000000	FBYTE22[R/W] B,H,W 00000000	FBYTE12[R/W] B,H,W 00000000	
00156C$_H$	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3 [R/W] B,H,W 000000-0	SSR3 [R/W] B,H,W 0--00011	ESCR3/(IBSR3) [R/W] B,H,W 00000000	Multi Function Serial I/F 3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001570$_H$	-/(RDR13/(TDR13))[R/W] H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
001574$_H$	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
001578$_H$	STMCR3[R/W] B,H,W 00000000 00000000		-/(SCSCR3/SFUR3) [R/W] B,H,W -------- -------- *3,*4		
00157C$_H$	-/(SCSTR33) [R/W] B,H,W -------- *3	-/(SCSTR23) [R/W] B,H,W -------- *3	-/(SCSTR13/SFLR13) [R/W] B,H,W -------- *3,*4	-/(SCSTR03/SFLR03) [R/W] B,H,W -------- *3,*4	
001580$_H$	-	-	-	-	
001584$_H$	-	-	-	TBYTE03[R/W] B,H,W 00000000	
001588$_H$	BGR3[R/W] H,W 00000000 00000000		-/(ISMK3)[R/W] B,H,W -------- *2	-/(ISBA3)[R/W] B,H,W -------- *2	
00158C$_H$	FCR13[R/W] B,H,W 00-00100	FCR03[R/W] B,H,W -0000000	FBYTE23[R/W] B,H,W 00000000	FBYTE13[R/W] B,H,W 00000000	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
001590_H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4 [R/W] B,H,W 000000-0	SSR4 [R/W] B,H,W 0--00011	ESCR4/(IBSR4) [R/W] B,H,W 00000000	Multi Function Serial I/F 4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset *3: Reserved because CSIO mode is not set immediately after reset *4: Reserved because LIN2.1 mode is not set immediately after reset
001594_H	-/(RDR14/(TDR14))[R/W] H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
001598_H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
$00159C_H$	STMCR4[R/W] B,H,W 00000000 00000000		-/(SCSCR4/SFUR4) [R/W] B,H,W -------- -------- *3,*4		
$0015A0_H$	-/(SCSTR34) [R/W] B,H,W -------- *3	-/(SCSTR24) [R/W] B,H,W -------- *3	-/(SCSTR14/SFLR14) [R/W] B,H,W -------- *3,*4	-/(SCSTR04/SFLR04) [R/W] B,H,W -------- *3,*4	
$0015A4_H$	-	-/(SCSFR24)[R/W] B,H,W -------- *3	-/(SCSFR14)[R/W] B,H,W -------- *3	-/(SCSFR04)[R/W] B,H,W -------- *3	
$0015A8_H$	-/(TBYTE34)[R/W] B,H,W -------- *3	-/(TBYTE24)[R/W] B,H,W -------- *3	-/(TBYTE14)[R/W] B,H,W -------- *3	TBYTE04[R/W] B,H,W 00000000	
$0015AC_H$	BGR4[R/W] H,W 00000000 00000000		-/(ISMK4)[R/W] B,H,W -------- *2	-/(ISBA4)[R/W] B,H,W -------- *2	
$0015B0_H$	FCR14[R/W] B,H,W 00-00100	FCR04[R/W] B,H,W -0000000	FBYTE24[R/W] B,H,W 00000000	FBYTE14[R/W] B,H,W 00000000	
$0015B4_H$ | $001FFC_H$	-	-	-	-	Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002000_H	CTRLR0[R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN 0 64msb
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008_H	INTR0[R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0[R/W] B,H,W -------- ----0000		-		
002010_H	IF1CREQ0[R/W] B,H,W 0------- 00000001		IF1CMSK0[R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20[R/W] B,H,W 11-11111 11111111		IF1MSK10[R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20[R/W] B,H,W 00000000 00000000		IF1ARB10[R/W] B,H,W 00000000 00000000		
$00201C_H$	IF1MCTR0[R/W] B,H,W 00000000 0---0000		-		
002020_H	IF1DTA10[R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10[R/W] B,H,W 00000000 00000000		IF1DTB20[R/W] B,H,W 00000000 00000000		
002028_H, $00202C_H$	-		-		
002030_H, 002034_H	Reserved (IF1 data mirror)				
002038_H, $00203C_H$	-		-		
002040_H	IF2CREQ0[R/W] B,H,W 0------- 00000001		IF2CMSK0[R/W] B,H,W -------- 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002044_H	IF2MSK20[R/W] B,H,W 11-11111 11111111		IF2MSK10[R/W] B,H,W 11111111 11111111		CAN 0 64msb
002048_H	IF2ARB20[R/W] B,H,W 00000000 00000000		IF2ARB10[R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0[R/W] B,H,W 00000000 0---0000		-		
002050_H	IF2DTA10[R/W] B,H,W 00000000 00000000		IF2DTA20[R/W] B,H,W 00000000 00000000		
002054_H	IF2DTB10[R/W] B,H,W 00000000 00000000		IF2DTB20[R/W] B,H,W 00000000 00000000		
002058_H, $00205C_H$	-		-		
002060_H, 002064_H	Reserved (IF2 data mirror)				
002068_H | $00207C_H$	-		-		
002080_H	TREQR20[R] B,H,W 00000000 00000000		TREQR10[R] B,H,W 00000000 00000000		
002084_H	TREQR40[R] B,H,W 00000000 00000000		TREQR30[R] B,H,W 00000000 00000000		
002088_H	-		-		
$00208C_H$	-		-		
002090_H	NEWDT20[R] B,H,W 00000000 00000000		NEWDT10[R] B,H,W 00000000 00000000		
002094_H	NEWDT40[R] B,H,W 00000000 00000000		NEWDT30[R] B,H,W 00000000 00000000		
002098_H	-		-		
$00209C_H$	-		-		
$0020A0_H$	INTPND20[R] B,H,W 00000000 00000000		INTPND10[R] B,H,W 00000000 00000000		
$0020A4_H$	INTPND40[R] B,H,W 00000000 00000000		INTPND30[R] B,H,W 00000000 00000000		
$0020A8_H$	-		-		
$0020AC_H$	-		-		
$0020B0_H$	MSGVAL20[R] B,H,W 00000000 00000000		MSGVAL10[R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40[R] B,H,W 00000000 00000000		MSGVAL30[R] B,H,W 00000000 00000000		
$0020B8_H$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$0020BC_H$	-		-		CAN 0 64msb
$0020C0_H$ | $0020FC_H$	-		-		
002100_H	CTRLR1[R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN1 64msb
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108_H	INTR1[R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1[R/W] B,H,W -------- ----0000		-		
002110_H	IF1CREQ1[R/W] B,H,W 0------- 00000001		IF1CMSK1[R/W] B,H,W -------- 00000000		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002114_H	IF1MSK21[R/W] B,H,W 11-11111 11111111		IF1MSK11[R/W] B,H,W 11111111 11111111		CAN 1 64msb
002118_H	IF1ARB21[R/W] B,H,W 00000000 00000000		IF1ARB11[R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1[R/W] B,H,W 00000000 0---0000		-		
002120_H	IF1DTA11[R/W] B,H,W 00000000 00000000		IF1DTA21[R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11[R/W] B,H,W 00000000 00000000		IF1DTB21[R/W] B,H,W 00000000 00000000		
002128_H, $00212C_H$	-		-		
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H, $00213C_H$	-		-		
002140_H	IF2CREQ1[R/W] B,H,W 0------- 00000001		IF2CMSK1[R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21[R/W] B,H,W 11-11111 11111111		IF2MSK11[R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21[R/W] B,H,W 00000000 00000000		IF2ARB11[R/W] B,H,W 00000000 00000000		
$00214C_H$	IF2MCTR1[R/W] B,H,W 00000000 0---0000		-		
002150_H	IF2DTA11[R/W] B,H,W 00000000 00000000		IF2DTA21[R/W] B,H,W 00000000 00000000		
002154_H	IF2DTB11[R/W] B,H,W 00000000 00000000		IF2DTB21[R/W] B,H,W 00000000 00000000		
002158_H, $00215C_H$	-		-		
002160_H, 002164_H	Reserved (IF2 data mirror)				
002168_H | $00217C_H$	-		-		
002180_H	TREQR21[R] B,H,W 00000000 00000000		TREQR11[R] B,H,W 00000000 00000000		
002184_H	TREQR41[R] B,H,W 00000000 00000000		TREQR31[R] B,H,W 00000000 00000000		
002188_H	-		-		
$00218C_H$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
002190_H	NEWDT21[R] B,H,W 00000000 00000000		NEWDT11[R] B,H,W 00000000 00000000		CAN 1 64msb
002194_H	NEWDT41[R] B,H,W 00000000 00000000		NEWDT31[R] B,H,W 00000000 00000000		
002198_H	-		-		
$00219C_H$	-		-		
$0021A0_H$	INTPND21[R] B,H,W 00000000 00000000		INTPND11[R] B,H,W 00000000 00000000		
$0021A4_H$	INTPND41[R] B,H,W 00000000 00000000		INTPND31[R] B,H,W 00000000 00000000		
$0021A8_H$	-		-		
$0021AC_H$	-		-		
$0021B0_H$	MSGVAL21[R] B,H,W 00000000 00000000		MSGVAL11[R] B,H,W 00000000 00000000		
$0021B4_H$	MSGVAL41[R] B,H,W 00000000 00000000		MSGVAL31[R] B,H,W 00000000 00000000		
$0021B8_H$	-		-		
$0021BC_H$	-		-		
$0021C0_H$ | $0021FC_H$	-		-		
002200_H	CTRLR2[R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN 2 64msb
002204_H	ERRCNT2 [R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208_H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
$00220C_H$	BRPER2[R/W] B,H,W -------- ----0000		-		
002210_H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		
002214_H	IF1MSK22[R/W] B,H,W 11-11111 11111111		IF1MSK12[R/W] B,H,W 11111111 11111111		
002218_H	IF1ARB22[R/W] B,H,W 00000000 00000000		IF1ARB12[R/W] B,H,W 00000000 00000000		
$00221C_H$	IF1MCTR2[R/W] B,H,W 00000000 0---0000		-		
002220_H	IF1DTA12[R/W] B,H,W 00000000 00000000		IF1DTA22[R/W] B,H,W 00000000 00000000		
002224_H	IF1DTB12[R/W] B,H,W 00000000 00000000		IF1DTB22[R/W] B,H,W 00000000 00000000		
002228_H, $00222C_H$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$002230_{H,}$ 002234_{H}	Reserved (IF1 data mirror)				CAN 2 64msb
$002238_{H,}$ $00223C_{H}$	-		-		
002240_{H}	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244_{H}	IF2MSK22[R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248_{H}	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
$00224C_{H}$	IF2MCTR2[R/W] B,H,W 00000000 0---0000		-		
002250_{H}	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254_{H}	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		
$002258_{H,}$ $00225C_{H}$	-		-		
$002260_{H,}$ 002264_{H}	Reserved (IF2 data mirror)				
002268_{H} | $00227C_{H}$	-		-		
002280_{H}	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284_{H}	TREQR42[R] B,H,W 00000000 00000000		TREQR32[R] B,H,W 00000000 00000000		
002288_{H}	-		-		
$00228C_{H}$	-		-		
002290_{H}	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294_{H}	NEWDT42[R] B,H,W 00000000 00000000		NEWDT32[R] B,H,W 00000000 00000000		
002298_{H}	-		-		
$00229C_{H}$	-		-		
$0022A0_{H}$	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
$0022A4_{H}$	INTPND42[R] B,H,W 00000000 00000000		INTPND32[R] B,H,W 00000000 00000000		
$0022A8_{H}$	-		-		

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
0022AC$_H$	-		-		CAN 2 64msb
0022B0$_H$	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
0022B4$_H$	MSGVAL42[R] B,H,W 00000000 00000000		MSGVAL32[R] B,H,W 00000000 00000000		
0022B8$_H$	-		-		
0022BC$_H$	-		-		
0022C0$_H$ | 0022FC$_H$	-	-	-	-	
002300$_H$	DFCTLR[R/W] B,H,W -0------ --------		-	DFSTR[R/W] B,H,W -----001	WorkFlash
002304$_H$	-	-	-	-	
002308$_H$	FLIFCTLR[R/W] B,H,W ---0--00	-	FLIFFER1[R/W] B,H,W --------	FLIFFER2[R/W] B,H,W --------	
00230C$_H$ | 002FFC$_H$	-	-	-	-	Reserved
003000$_H$	SEEARX[R] B,H,W -0000000 00000000		DEEARX[R] B,H,W -0000000 00000000		XBS RAM ECC control register
003004$_H$	EECSRX[R/W] B,H,W ----00-0	-	EFEARX[R/W] B,H,W -0000000 00000000		
003008$_H$	-	EFECRX[R/W] B,H,W -------0 00000000 00000000			
00300C$_H$	TEAR0X[R] B,H,W 000----- -------- -0000000 00000000				XBS RAM diagnosis register
003010$_H$	TEAR1X[R] B,H,W 000----- -------- -0000000 00000000				
003014$_H$	TEAR2X[R] B,H,W 000----- -------- -0000000 00000000				
003018$_H$	TAEARX[R/W] B,H,W -1011111 11111111		TASARX[R/W] B,H,W -0000000 00000000		
00301C$_H$	TFECRX[R/W] B,H,W ----0000	TICRX[R/W] B,H,W ----0000	TTCRX[R/W] B,H,W ------00 00001100		
003020$_H$	TSRCRX[R/W] B,H,W 0-------	-	-	TKCCRX[R/W] B,H,W 00----00	

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003024_H	SEEARA[R] B,H,W --000000 00000000		DEEARA[R] B,H,W --000000 00000000		Backup RAM ECC control register
003028_H	EECSRA[R/W] B,H,W ----00-0	-	EFEARA[R/W] B,H,W --000000 00000000		
$00302C_H$	-	EFECRA[R/W] B,H,W -------0 00000000 00000000			
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				Backup RAM diagnosis register
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA[R/W] B,H,W ----0000	TICRA[R/W] B,H,W ----0000	TTCRA[R/W] B,H,W ------00 00001100		
003044_H	TSRCRA[R/W] B,H,W 0-------	-	-	TKCCRA[R/W] B,H,W 00----00	
003048_H | $0030FC_H$	-	-	-	-	Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		Bus diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0[R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1[R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2[R] W 00000000 00000000 00000000 00000000				
003114_H	-		BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--0000 00000000		
$00311C_H$	-				
003120_H	BUSADR3[R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4[R] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
003128_H | $003FFC_H$	-	-	-	-	Reserved
004000_H | $005FFC_H$	Backup RAM				Backup RAM area
006000_H | $00CFFC_H$	-	-	-	-	Reserved
$00D000_H$	CIF0[R] W 00000100 11111111 01011011 11111111				FlexRay CIF
$00D004_H$	CIF1[R/W] W 00000000 -------0 -0000000 --------				
$00D008_H$ | $00D00C_H$	-	-	-	-	Reserved
$00D010_H$	-				FlexRay GIF
$00D014_H$	-				
$00D018_H$	-	-	-	-	
$00D01C_H$	LCK[R/W] W -------- -------- -------- 00000000				
$00D020_H$	EIR[R/W] W -----000 -----000 ----0000 00000000				FlexRay INT
$00D024_H$	SIR[R/W] W ------00 ------00 00000000 00000000				
$00D028_H$	EILS[R/W] W -----000 -----000 ----0000 00000000				
$00D02C_H$	SILS[R/W] W ------11 ------11 11111111 11111111				
$00D030_H$	EIES[R/W] W -----000 -----000 ----0000 00000000				
$00D034_H$	EIER[R/W] W -----000 -----000 ----0000 00000000				
$00D038_H$	SIES[R/W] W ------00 ------00 00000000 00000000				
$00D03C_H$	SIER[R/W] W ------00 ------00 00000000 00000000				
$00D040_H$	ILE[R/W] W -------- -------- -------- ------00				
$00D044_H$	T0C[R/W] W --000000 00000000 -0000000 ------00				
$00D048_H$	T1C[R/W] W --000000 00000010 -------- ------00				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D04C_H$	STPW1[R/W] W --000000 00000000 --000000 -0000000				FlexRay INT
$00D050_H$	STPW2[R] W -----000 00000000 -----000 00000000				
$00D054_H$ | $00D07C_H$	-	-	-	-	Reserved
$00D080_H$	SUCC1[R/W] W ----1100 01000000 00010-00 1---0000				FlexRay SUC
$00D084_H$	SUCC2[R/W] W ----0001 ---00000 00000101 00000100				
$00D088_H$	SUCC3[R/W] W -------- -------- -------- 00010001				
$00D08C_H$	NEMC[R/W] W -------- -------- -------- ----0000				FlexRay NEM
$00D090_H$	PRTC1[R/W] W 000010-0 01001100 0000-110 00110011				FlexRay PRT
$00D094_H$	PRTC2[R/W] W --001111 00101101 --001010 --001110				
$00D098_H$	MHDC[R/W] W ---00000 00000000 -------- -0000000				FlexRay MHD
$00D09C_H$	-				Reserved
$00D0A0_H$	GTUC1[R/W] W -------- ----0000 00000010 10000000				FlexRay GTU
$00D0A4_H$	GTUC2[R/W] W -------- ----0010 --000000 00001010				
$00D0A8_H$	GTUC3[R/W] W -0000010 -0000010 00000000 00000000				
$00D0AC_H$	GTUC4[R/W] W --000000 00001000 --000000 00000111				
$00D0B0_H$	GTUC5[R/W] W 00001110 ---00000 00000000 00000000				
$00D0B4_H$	GTUC6[R/W] W -----000 00000010 -----000 00000000				
$00D0B8_H$	GTUC7[R/W] W ------00 00000010 ------00 00000100				
$00D0BC_H$	GTUC8[R/W] W ---00000 00000000 -------- --000010				
$00D0C0_H$	GTUC9[R/W] W -------- ------00 ---00001 --000001				
$00D0C4_H$	GTUC10[R/W] W -----000 00000010 --000000 00000101				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D0C8_H$	GTUC11[R/W] W -----000 -----000 ------00 ------00				FlexRay GTU
$00D0CC_H$ | $00D0FC_H$	-				Reserved
$00D100_H$	CCSV[R] W --000000 00010000 -100--00 00000000				FlexRay SUC
$00D104_H$	CCEV[R] W -------- -------- ---00000 00--0000				
$00D108_H$ $00D10C_H$	-				Reserved
$00D110_H$	SCV[R] W -----000 00000000 -----000 00000000				FlexRay GTU
$00D114_H$	MTCCV[R] W -------- --000000 --000000 00000000				
$00D118_H$	RCV[R] W				
	-------- -------- ----0000 00000000				
$00D11C_H$	OCV[R] W -------- -----000 00000000 00000000				
$00D120_H$	SFS[R] W -------- ----0000 00000000 00000000				
$00D124_H$	SWNIT[R] W -------- -------- ----0000 00000000				
$00D128_H$	ACS[R/W] W -------- -------- ---00000 ---00000				
$00D12C_H$	-				
$00D130_H$	ESID1[R] W -------- -------- 00----00 00000000				
$00D134_H$	ESID2[R] W -------- -------- 00----00 00000000				
$00D138_H$	ESID3[R] W -------- -------- 00----00 00000000				
$00D13C_H$	ESID4[R] W -------- -------- 00----00 00000000				
$00D140_H$	ESID5[R] W -------- -------- 00----00 00000000				
$00D144_H$	ESID6[R] W -------- -------- 00----00 00000000				
$00D148_H$	ESID7[R] W -------- -------- 00----00 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D14C_H$	ESID8[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D150_H$	ESID9[R] W -------- -------- 00----00 00000000				
$00D154_H$	ESID10[R] W -------- -------- 00----00 00000000				
$00D158_H$	ESID11[R] W -------- -------- 00----00 00000000				
$00D15C_H$	ESID12[R] W -------- -------- 00----00 00000000				
$00D160_H$	ESID13[R] W -------- -------- 00----00 00000000				
$00D164_H$	ESID14[R] W -------- -------- 00----00 00000000				
$00D168_H$	ESID15[R] W -------- -------- 00----00 00000000				
$00D16C_H$	-				
$00D170_H$	OSID1[R] W -------- -------- 00----00 00000000				
$00D174_H$	OSID2[R] W -------- -------- 00----00 00000000				
$00D178_H$	OSID3[R] W -------- -------- 00----00 00000000				
$00D17C_H$	OSID4[R] W -------- -------- 00----00 00000000				
$00D180_H$	OSID5[R] W -------- -------- 00----00 00000000				
$00D184_H$	OSID6[R] W -------- -------- 00----00 00000000				
$00D188_H$	OSID7[R] W -------- -------- 00----00 00000000				
$00D18C_H$	OSID8[R] W -------- -------- 00----00 00000000				
$00D190_H$	OSID9[R] W -------- -------- 00----00 00000000				
$00D194_H$	OSID10[R] W -------- -------- 00----00 00000000				
$00D198_H$	OSID11[R] W -------- -------- 00----00 00000000				
$00D19C_H$	OSID12[R] W -------- -------- 00----00 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D1A0_H$	OSID13[R] W -------- -------- 00----00 00000000				FlexRay GTU
$00D1A4_H$	OSID14[R] W -------- -------- 00----00 00000000				
$00D1A8_H$	OSID15[R] W -------- -------- 00----00 00000000				
$00D1AC_H$	-				Reserved
$00D1B0_H$	NMV1[R] W 00000000 00000000 00000000 00000000				FlexRay NEM
$00D1B4_H$	NMV2[R] W 00000000 00000000 00000000 00000000				
$00D1B8_H$	NMV3[R] W 00000000 00000000 00000000 00000000				
$00D1BC_H$ | $00D2FC_H$	-				Reserved
$00D300_H$	MRC[R/W] W -----001 10000000 00000000 00000000				FlexRay MHD
$00D304_H$	FRF[R/W] W				
	-------1 10000000 ---00000 00000000				
$00D308_H$	FRFM[R/W] W -------- -------- ---00000 000000--				
$00D30C_H$	FCL[R/W] W -------- -------- -------- 10000000				
$00D310_H$	MHDS[R/W] W -0000000 -0000000 -0000000 00000000				
$00D314_H$	LDTS[R] W -----000 00000000 -----000 00000000				
$00D318_H$	FSR[R] W -------- -------- 00000000 -----000				
$00D31C_H$	MHDF[R/W] W -------- -------- -------0 00000000				
$00D320_H$	TXRQ1[R] W 00000000 00000000 00000000 00000000				
$00D324_H$	TXRQ2[R] W 00000000 00000000 00000000 00000000				
$00D328_H$	TXRQ3[R] W 00000000 00000000 00000000 00000000				
$00D32C_H$	TXRQ4[R] W 00000000 00000000 00000000 00000000				

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D330_H$	NDAT1[R] W 00000000 00000000 00000000 00000000				FlexRay MHD
$00D334_H$	NDAT2[R] W 00000000 00000000 00000000 00000000				
$00D338_H$	NDAT3[R] W 00000000 00000000 00000000 00000000				
$00D33C_H$	NDAT4[R] W 00000000 00000000 00000000 00000000				
$00D340_H$	MBSC1[R] W 00000000 00000000 00000000 00000000				
$00D344_H$	MBSC2[R] W 00000000 00000000 00000000 00000000				
$00D348_H$	MBSC3[R] W 00000000 00000000 00000000 00000000				
$00D34C_H$	MBSC4[R] W 00000000 00000000 00000000 00000000				
$00D350_H$ | $00D3EC_H$	-				Reserved
$00D3F0_H$	CREL[R] W 00010000 00111001 00000010 00000110				FlexRay GIF
$00D3F4_H$	ENDN[R] W 10000111 01100101 01000011 00100001				
$00D3F8_H$ | $00D3FC_H$	-				Reserved
$00D400_H$ | $00D4FC_H$	WRDSn[1-64][R/W] W 00000000 00000000 00000000 00000000				FlexRay IBF
$00D500_H$	WRHS1[R/W] W --000000 -0000000 -----000 00000000				
$00D504_H$	WRHS2[R/W] W -------- -0000000 -----000 00000000				
$00D508_H$	WRHS3[R/W] W -------- -------- -----000 00000000				
$00D50C_H$	-				
$00D510_H$	IBCM[R/W] W -------- ------00 -------- -----000				
$00D514_H$	IBCR[R/W] W 0------- -0000000 0------- -0000000				
$00D518_H$ | $00D5FC_H$	-				Reserved

Address	Address offset value/Register name				Block
	+0	+1	+2	+3	
$00D600_H$ | $00D6FC_H$	RDDSn[1-64][R] W 00000000 00000000 00000000 00000000				FlexRay OBF
$00D700_H$	RDHS1[R] W --000000 -0000000 -----000 00000000				
$00D704_H$	RDHS2[R] W -0000000 -0000000 -----000 00000000				
$00D708_H$	RDHS3[R] W --000000 --000000 -----000 00000000				
$00D70C_H$	MBS[R] W --000000 --000000 00-00000 00000000				
$00D710_H$	OBCM[R/W] W -------- ------00 -------- ------00				
$00D714_H$	OBCR[R/W] W -------- -0000000 0-----00 -0000000				
$00D718_H$ | $00D7FC_H$	-				Reserved
$00D800_H$ | $00EFFC_H$	-				Reserved
$00F000_H$ | $00FEFC_H$	-				Reserved [S]
$00FF00_H$	DSUCR[R/W] B,H,W -------- -------0		-	-	OCDU [S]
$00FF04_H$ | $00FF0C_H$	-	-	-	-	Reserved [S]
$00FF10_H$	PCSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR[R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ | $00FFF4_H$	-	-	-	-	Reserved [S]
$00FFF8_H$	EDIR1[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0[R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]: It is a system register. The illegal instruction exception (data access error) is generated when reading and writing to these registers in the user mode.

11. Interrupt Vector Table

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN[*1]	Interrupt request batch read target
	Decimal	Hexadecimal					
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-	-
Instruction access protection violation exception	6	06	-	$3E4_H$	$000FFFE4_H$	-	-
Data access protection violation exception	7	07	-	$3E0_H$	$000FFFE0_H$	-	-
Data access error interrupts	8	08	-	$3DC_H$	$000FFFDC_H$	-	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-	-
NMI request Error generation at internal bus diagnosis RAM double-bit error Backup RAM double-bit error RDC abnormality [*5]	15	0F	$15(F_H)$ Fixed	$3C0_H$	$000FFFC0_H$	-	○
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0	-
Reload timer 0 / 1	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1	○
Reload timer 2 / 3	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2	○
Multifunction serial interface ch0 (reception completed) / Multifunction serial interface ch0 (status)	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3[*2]	○
Multifunction serial interface ch0 (transmission completed)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4	-
Multifunction serial interface ch1 (reception completed) / Multifunction serial interface ch1 (status)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5[*2]	○
Multifunction serial interface ch1 (transmission completed)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6	-
Multifunction serial interface ch2 (reception completed) / Multifunction serial interface ch2 (status)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7[*2]	○
Multifunction serial interface ch2 (transmission completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8	-

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN[*1]	Interrupt request batch read target
	Decimal	Hexadecimal					
Multifunction serial interface ch 3 (reception completed) / Multifunction serial interface ch3 (status)	25	19	ICR09	398_H	$000FFF98_H$	9[*2]	○
Multifunction serial interface ch3 (transmission completed)	26	1A	ICR10	394_H	$000FFF94_H$	10	-
Multifunction serial interface ch 4 (reception completed) / Multifunction serial interface ch4 (status)	27	1B	ICR11	390_H	$000FFF90_H$	11[*2]	○
Multifunction serial interface ch4 (transmission completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12	-
CAN 0	29	1D	ICR13	388_H	$000FFF88_H$	-	-
CAN 1	30	1E	ICR14	384_H	$000FFF84_H$	-	-
CAN 2 / FlexRay 0	31	1F	ICR15	380_H	$000FFF80_H$	-	○
FlexRay 1	32	20	ICR16	$37C_H$	$000FFF7C_H$	-	-
FlexRay timer 0	33	21	ICR17	378_H	$000FFF78_H$	-	-
FlexRay timer 1	34	22	ICR18	374_H	$000FFF74_H$	-	-
RAM diagnosis completed RAM initialization completed Error generation at RAM diagnosis Backup RAM diagnosis completed Backup RAM initialization completed Error generation at Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-	○
Main timer/PLL timer/PLL gear for FlexRay/PLL alarm for FlexRay	36	24	ICR20	$36C_H$	$000FFF6C_H$	20[*3]	○
Clock calibration unit (CR oscillation)	37	25	ICR21	368_H	$000FFF68_H$	-	-
U/D counter 0 / 1	38	26	ICR22	364_H	$000FFF64_H$	22	○
Free-run timer 0 (0 detection)/ (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23	○
Free-run timer 1 (0 detection)/ (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24	○
Free-run timer 2 (0 detection)/ (compare clear) PPG 0 / 1 / 2 / 3	41	29	ICR25	358_H	$000FFF58_H$	25	○
Free-run timer 3 (0 detection)/ (compare clear)	42	2A	ICR26	354_H	$000FFF54_H$	26	○
Free-run timer 4 (0 detection)/ (compare clear)	43	2B	ICR27	350_H	$000FFF50_H$	27	○
Free-run timer 5 (0 detection)/ (compare clear) PPG 4 / 5 / 6 / 7	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28	○
ICU 0 (fetching) / ICU 1 (fetching) PPG 8 / 9 / 10 / 11	45	2D	ICR29	348_H	$000FFF48_H$	29	○

Interrupt factor	Interrupt number		Interrupt level	Offset	TBR default address	RN*1	Interrupt request batch read target
	Decimal	Hexadecimal					
ICU 2 (fetching) / ICU 3 (fetching) PPG 12 / 13 / 14 / 15	46	2E	ICR30	344_H	$000FFF44_H$	30	O
ICU 4 (fetching)) / ICU 5 (fetching) PPG 16 / 17 / 18 / 19	47	2F	ICR31	340_H	$000FFF40_H$	31	O
ICU 6 (fetching) / ICU 7 (fetching) PPG 20 / 21 / 22 / 23	48	30	ICR32	$33C_H$	$000FFF3C_H$	32	O
OCU 0 (match) / OCU 1 (match)	49	31	ICR33	338_H	$000FFF38_H$	33	O
OCU 2 (match) / OCU 3 (match)	50	32	ICR34	334_H	$000FFF34_H$	34	O
OCU 4 (match) / OCU 5 (match)	51	33	ICR35	330_H	$000FFF30_H$	35	O
OCU 6 (match) / OCU 7 (match)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36	O
OCU 8 (match) / OCU 9 (match)	53	35	ICR37	328_H	$000FFF28_H$	37	O
OCU 10 (match) / OCU 11 (match)	54	36	ICR38	324_H	$000FFF24_H$	38	O
WG dead timer underflow 0 / 1/ 2 WG dead timer reload 0 / 1/ 2 WG DTTI 0	55	37	ICR39	320_H	$000FFF20_H$	39	O
WG dead timer underflow 3 / 4 / 5 WG dead timer reload 3 / 4 / 5 WG DTTI 1	56	38	ICR40	$31C_H$	$000FFF1C_H$	40	O
AD converter 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	57	39	ICR41	318_H	$000FFF18_H$	41	O
AD converter 8 / 9 / 10 / 11 / 12 / 13 / 14 / 15	58	3A	ICR42	314_H	$000FFF14_H$	42	O
AD converter 16 / 17 / 18 / 19 / 20 / 21 / 22 / 23	59	3B	ICR43	310_H	$000FFF10_H$	43	O
Base timer 0 IRQ 0/ base timer 0 IRQ 1	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44	O
Base timer 1 IRQ 0/ base timer 1 IRQ 1	61	3D	ICR45	308_H	$000FFF08_H$	45	O
DMAC 0 / 1 / 2 / 3 / 4 / 5 / 6 / 7	62	3E	ICR46	304_H	$000FFF04_H$	-	O
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-	-
System reserved (Used for REALOS *4.)	64	40	-	$2FC_H$	$000FFEFC_H$	-	-
System reserved (Used for REALOS *4.)	65	41	-	$2F8_H$	$000FFEF8_H$	-	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-	-

*1 :Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (resource number) is assigned.

*2 :The multi-function serial interface status does not support DMA transfer caused by I^2C reception.

*3 :"PLL gear for FlexRay" and "PLL alarm for FlexRay" do not support DMA transfer.

*4 REALOS is a trademark of Cypress Semiconductor.

*5 : For RDC, the MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC have corresponding functions.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1 ,*2	V_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	
Analog power supply voltage*1, *2	AV_{CC}	V_{SS}-0.3	V_{SS}+6.0	V	Avcc ≤ Vcc
Analog reference voltage*1	AVRH	V_{SS}-0.3	V_{SS}+6.0	V	AVRH ≤ AV_{CC}
Input voltage*1	V_I	V_{SS}-0.3	V_{CC}+0.3	V	
Analog pin input voltage*1	V_{IA}	V_{SS}-0.3	V_{CC}+0.3	V	
Output voltage*1	V_O	V_{SS}-0.3	V_{CC}+0.3	V	
Maximum clamp current	I_{CLAMP}	-	4	mA	*9
Total maximum clamp current	$\Sigma\|I_{CLAMP}\|$	-	20	mA	*9
"L" level maximum output current*3	I_{OL1}	-	7	mA	When setting to 2mA*6
	I_{OL2}	-	14	mA	When setting to 4mA*7
	I_{OL3}	-	17.5	mA	When setting to 5mA*8
"L" level average output current*4	I_{OLAV1}	-	2	mA	When setting to 2mA*6
	I_{OLAV2}	-	4	mA	When setting to 4mA*7
	I_{OLAV3}	-	5	mA	When setting to 5mA*8
"L" level total output current*5	ΣI_{OL}	-	50	mA	*6
"H" level maximum output current*3	I_{OH1}	-	-7	mA	When setting to 2mA*6
	I_{OH2}	-	-14	mA	When setting to 4mA*7
	I_{OH3}	-	-17.5	mA	When setting to 5mA*8
"H" level average output current*4	I_{OHAV1}	-	-2	mA	When setting to 2mA*6
	I_{OHAV2}	-	-4	mA	When setting to 4mA*7
	I_{OHAV3}	-	-5	mA	When setting to 5mA*8
"H" level total output current*5	ΣI_{OH}	-	-50	mA	*6
Power consumption	P_D	-	690	mW	
Operating temperature	T_A	-40	+125	°C	*10,*11
Storage temperature	Tstg	-55	+150	°C	

*1: These parameters are based on the condition that V_{SS}=AV_{SS} =0.0V.

*2: Caution must be taken that AV_{CC} does not exceed V_{CC}.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Corresponding pins: General-purpose ports

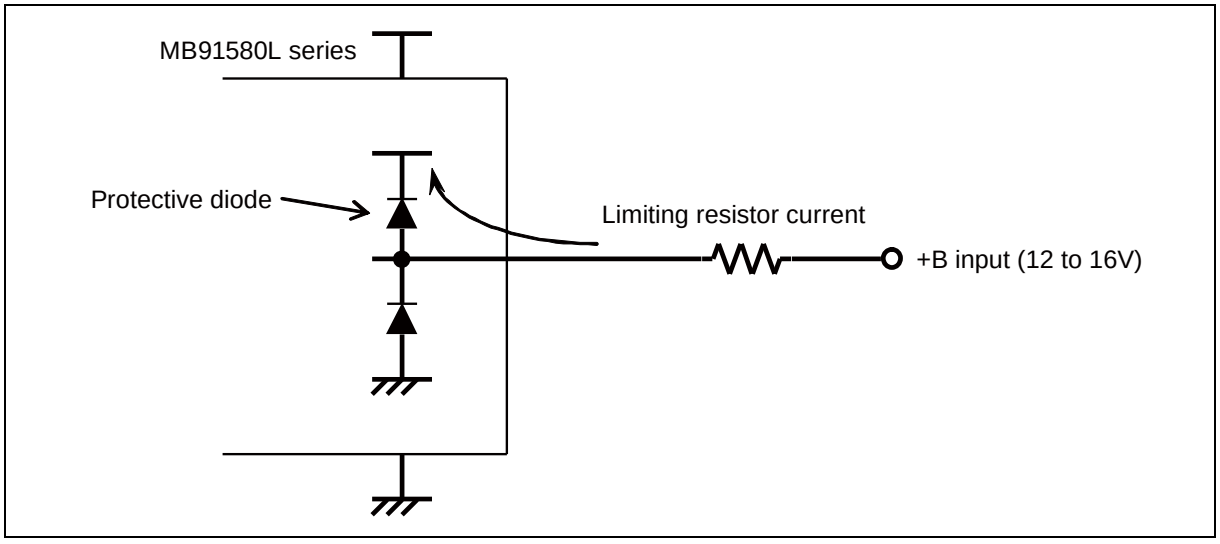
*7: Corresponding pins: General-purpose ports of P003 to P007, P010

*8: Corresponding pins: General-purpose ports other than those of P003 to P007, P010

*9: ● Corresponding pins: General-purpose ports

- Use the devices within recommended operating conditions.
- Use the devices with direct voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low-power consumption modes, the + B input potential can increase the potential at the V_{CC} pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Sample recommended circuit



*10:To use this product at T_A=125°C, equip this on a multilayer board with four or more layers.
To equip this on a single-layer board, change the operating conditions (operating frequency, power supply voltage, etc) to use this at the power consumption P_D=500mW or lower, or use this at T_A=110°C or lower.

*11: When it is used exceeding T_A=125°C, contact your sales representative.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

12.2 Recommended operating conditions

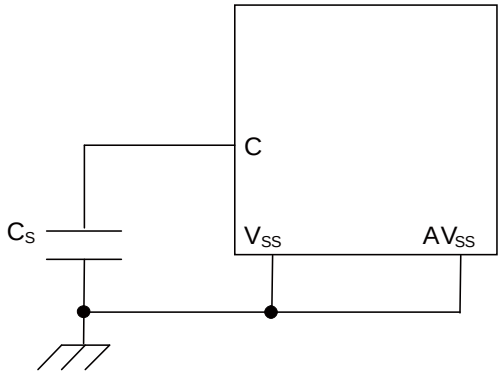
(V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	4.5	5.5	V	Recommended operation guarantee range
	AV_{CC}	4.5	5.5	V	
	V_{CC}	3.7	5.5	V	Operation guarantee range
	AV_{CC}	3.7	5.5	V	
Smoothing capacitor*1	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+125	°C	*2

*1: For connection of smoothing capacitor C_S, see the figure below.

*2: When it is used exceeding T_A=125°C, contact your sales representative.

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

12.3 DC characteristics

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	When CMOS schmitt input level is selected	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH2}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	When Automotive input level is selected	0.8 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH3}	P003 to P007, P010	When FlexRay input level is selected	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH4}	RSTX, NMIX	-	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH5}	MD0, MD1	-	0.7 × V_{CC}	-	V_{CC}+0.3	V	
	V_{IH6}	DEBUGIF	-	2.0	-	V_{CC}+0.3	V	

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	When CMOS schmitt input level is selected	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL2}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	When Automotive input level is selected	Vss-0.3	-	0.5 × V_{CC}	V	
	V_{IL3}	P003 to P007, P010	When FlexRay input level is selected	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL4}	RSTX, NMIX	-	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL5}	MD0, MD1	-	Vss-0.3	-	0.3 × V_{CC}	V	
	V_{IL6}	DEBUGIF	-	Vss-0.3	-	0.8	V	

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(T_A: Recommended operating conditions, Vcc=5.0V±10%,V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OH}=-2.0mA	Vcc-0.5	-	Vcc	V	
	V_{OH2}	P003 to P007, P010	Vcc=4.5V I_{OH}=-4.0mA	Vcc-0.5	-	Vcc	V	When FlexRay is selected
	V_{OH3}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OH}=-5.0mA	Vcc-0.5	-	Vcc	V	

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OL}=2.0mA	0	-	0.4	V	
	V_{OL2}	P003 to P007, P010	Vcc=4.5V I_{OL}=4.0mA	0	-	0.4	V	When FlexRay is selected
	V_{OL3}	P000 to P002, P011 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	Vcc=4.5V I_{OL}=5.0mA	0	-	0.4	V	
	V_{OL4}	P001,P002, P021,P022, P025,P026, P073,P074, P076,P077, P127,P130	Vcc=4.5V I_{OL}=3.0mA	0	-	0.4	V	I^2C shared pin (when I^2C is selected)

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value				Unit
				Min	Typ	Max	Min	
"L" level output voltage	V_{OL5}	DEBUGIF	Vcc=2.7V I_{OL}=25.0mA	0	-	0.25	V	
Input Leak Current	I_{IL}	All input pins	Vcc= AV_{CC}=5.5V $V_{SS} < V_I < V_{CC}$	-5	-	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	-	25	-	100	kΩ	
	R_{UP2}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P042, P043 to P047*, P050 to P057*, P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P134, P136 to P137	When pull-up resistance is selected	25	-	100	kΩ	
Input Capacitor	C_{IN}	Other than VCC, VSS, AVCC, AVSS, C	-	-	5	15	pF	

*: Only available with MB91F585LB/F586LB/F587LB, MB91F585LD/F586LD/F587LD

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	VCC5	Normal operations F_{CP}=128MHz, F_{CPP}=32MHz	-	85	110	mA	*1, *3 RDC=OFF, FlexRay =ON
				-	82	105	mA	*1, *3 RDC=ON, FlexRay =OFF
				-	85	110	mA	*2, *4 FlexRay =ON
				-	79	104	mA	*2, *4 FlexRay =OFF
			Normal operations F_{CP}=80MHz, F_{CPP}=40MHz	-	69	91	mA	*1, *3 RDC=OFF, FlexRay =ON
				-	67	89	mA	*1, *3 RDC=ON, FlexRay =OFF
				-	69	91	mA	*2, *4 FlexRay =ON
				-	64	87	mA	*2, *4 FlexRay =OFF
			Flash write	-	100	125	mA	*1, *3, *5
			F_{CP}=128MHz, F_{CPP}=32MHz	-	100	125	mA	*2, *4, *5
			Flash erase	-	100	125	mA	*1, *3, *5
			F_{CP}=128MHz, F_{CPP}=32MHz	-	100	125	mA	*2, *4, *5

*1: MB91F585LA/F586LA/F587LA

*2: MB91F585LB/F586LB/F587LB

*3: MB91F585LC/F586LC/F587LC

*4: MB91F585LD/F586LD/F587LD

*5: This series has 2 types of flash; main flash and WorkFlash; however, this is the specification when only one of those is written/erased.

(T_A: Recommended operating conditions, Vcc=5.0V±10%, V_{SS}= AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS}	VCC5	CPU sleep F_{CP}=128MHz, F_{CPP}=32MHz	-	46	68	mA	*1, *2, *3, *4
	I_{CCBS}		Bus sleep F_{CP}=128MHz, F_{CPP}=32MHz	-	31	54	mA	*1, *2, *3, *4
	I_{CCT}		Clock mode 4MHz source oscillation	-	1.2	1.8	mA	When using external clock*6 T_A=25°C, *1, *2, *3, *4
				-	2.7	3.3	mA	When using crystal T_A=25°C, *1, *2, *3, *4
	I_{CCTS}		Clock mode shutdown 4MHz source oscillation	-	0.7	0.8	mA	When using external clock*6 T_A=25°C, *3, *4
				-	2.2	2.3	mA	When using crystal T_A=25°C, *3, *4
				-	0.3	0.4	mA	When using external clock*6 T_A=25°C, *1, *2
				-	1.8	1.9	mA	When using crystal T_A=25°C, *1, *2
	I_{CCH}		STOP mode	-	1.0	1.6	mA	T_A=25°C, *3, *4
				-	0.6	1.1	mA	T_A=25°C, *1, *2
	I_{CCHS}		STOP mode shutdown	-	0.5	0.6	mA	T_A=25°C, *3, *4
				-	0.1	0.2	mA	T_A=25°C, *1, *2

*1: MB91F585LA/F586LA/F587LA

*2: MB91F585LB/F586LB/F587LB

*3: MB91F585LC/F586LC/F587LC

*4: MB91F585LD/F586LD/F587LD

*6: The power supply current is the current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

12.4 AC characteristics

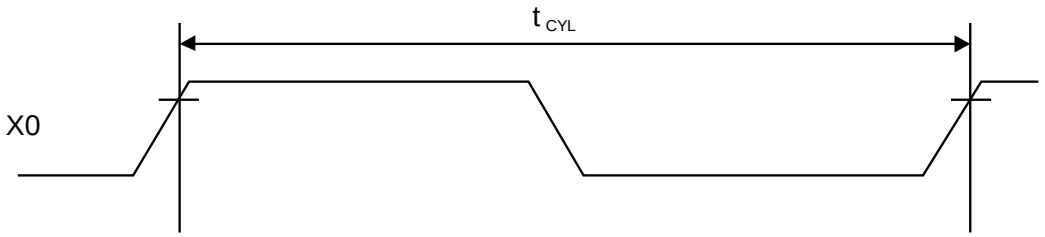
12.4.1 Main Clock Timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	4	-	20	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	50	-	250	ns	
Internal operating clock frequency*	F_{CP}	-	-	-	-	128	MHz	CPU clock
	F_{CPP}	-	-	-	-	40	MHz	Peripheral bus clock
	F_{CPT}	-	-	-	-	40	MHz	External bus clocks
Internal operating clock cycle time*	t_{CP}	-	-	7.82	-	-	ns	CPU clock
	t_{CPP}	-	-	25	-	-	ns	Peripheral bus clock
	t_{CPT}	-	-	25	-	-	ns	External bus clocks
CAN PLL jitter (during lock)	t_{PJ}	-	-	-10	-	+10	ns	
Built-in CR oscillation frequency	F_{CCR}	-	-	50	100	150	kHz	

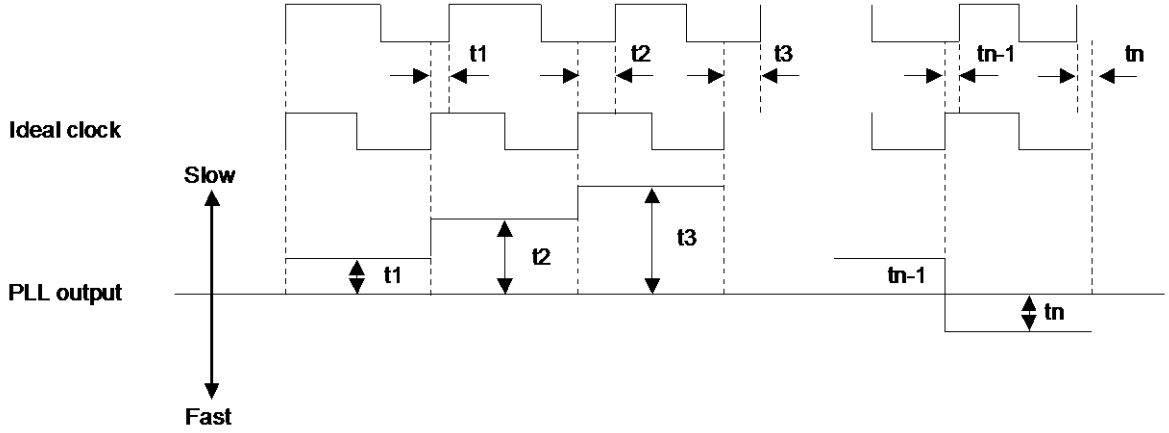
*: The maximum/minimum value is defined when using the main clock and PLL clock.

X0,X1 clock timing

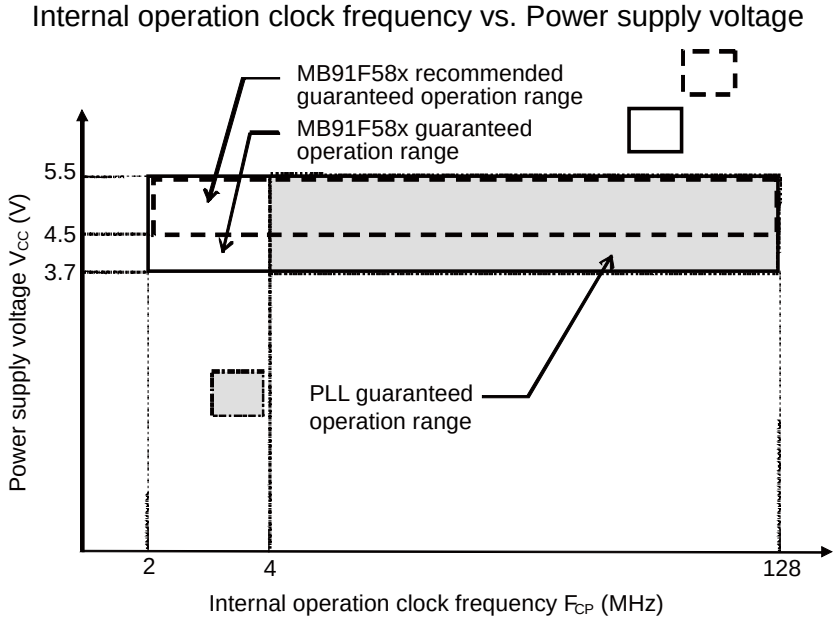


CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



Guaranteed operation range

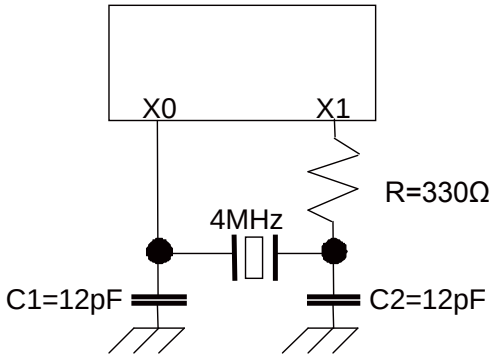


Note: The CPU will be reset at the power supply voltage of the low-voltage detection setting voltage or less.

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency								
		Main clock	PLL clock							
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	...	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	80MHz	...	128MHz

Example of oscillation circuit

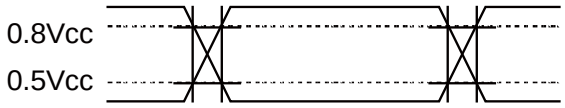


Note: If it is impossible to start the oscillation within or equal to 20ms when starting from the oscillation stop state, the clock supervisor performs a detection of oscillation stop and moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms.
In addition, when configuring the oscillator circuit, it is recommended to ask matching evaluation of the circuit to oscillator manufacturers for the design.

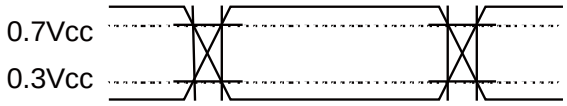
AC characteristics are specified by the following measurement reference voltage values.

Input Signal Waveform

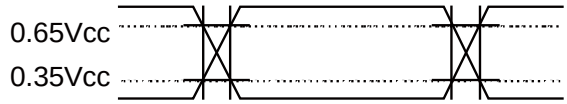
Hysteresis Input Pin (Automotive)



Hysteresis Input Pin (CMOS schmitt)



Hysteresis Input Pin (FlexRay)



Output Signal Waveform

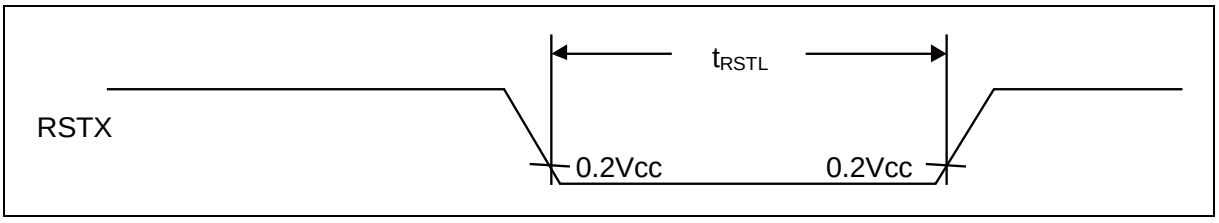
Output Pin

12.4.2 Reset input

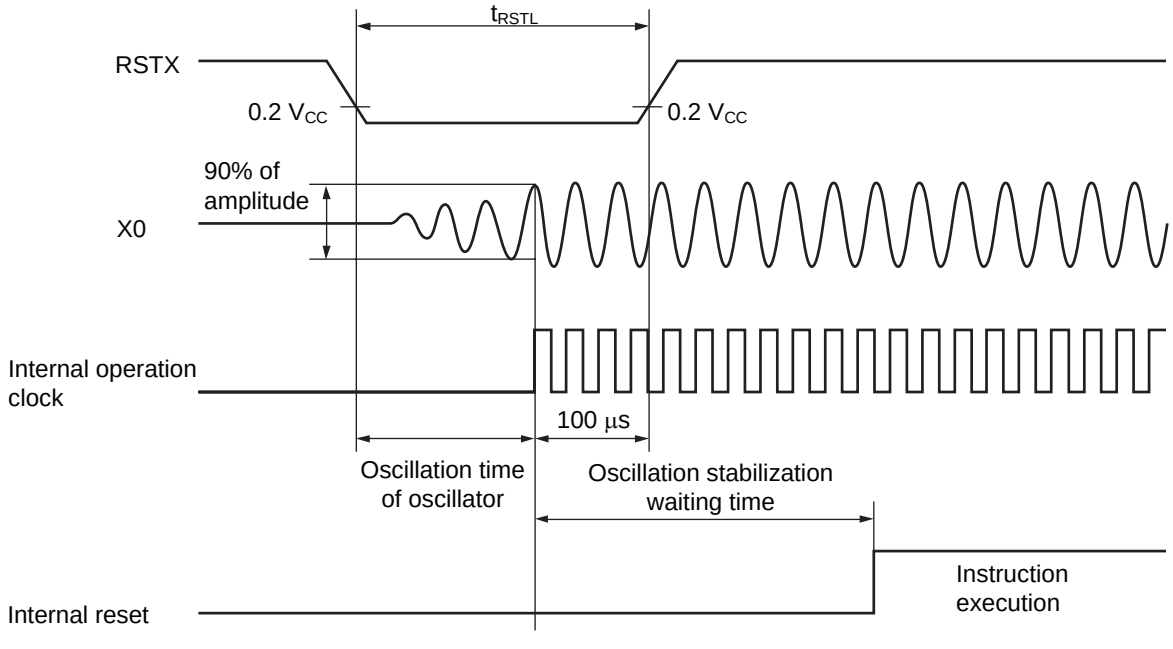
(T_A: Recommended operating conditions, Vcc =5.0V±10%, Vss=AVss=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	-	10	-	µs	During normal operation
				Oscillation time of oscillator * +0.1	-	ms	At Stop mode
				100	-	µs	At Clock mode
Width for reset input removal				1	-	µs	

*:The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.



In Stop mode



12.4.3 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	-	VCC5	-	2.1	2.3	2.5	V	When turning on power
Level detection hysteresis width	-	VCC5	-	-	-	125	mV	During voltage drop
Level detection time	-	-	-	-	-	30	µs	*1
Slope detection undetected standard	-	VCC5	V_{CC}= at level detection release level	-	-	4	mV/µs	*2
Power off time	t_{OFF}	VCC5	-	50	-	-	ms	*3

*1: If the fluctuation of the power supply is faster than the low-voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this standard or less, it is possible to suppress the slope detection. This is the standard when the power supply fluctuation is stable.

*3: This time is to start the slope detection at next power on after power down and internal charge loss.

12.4.4 Multi-function Serial

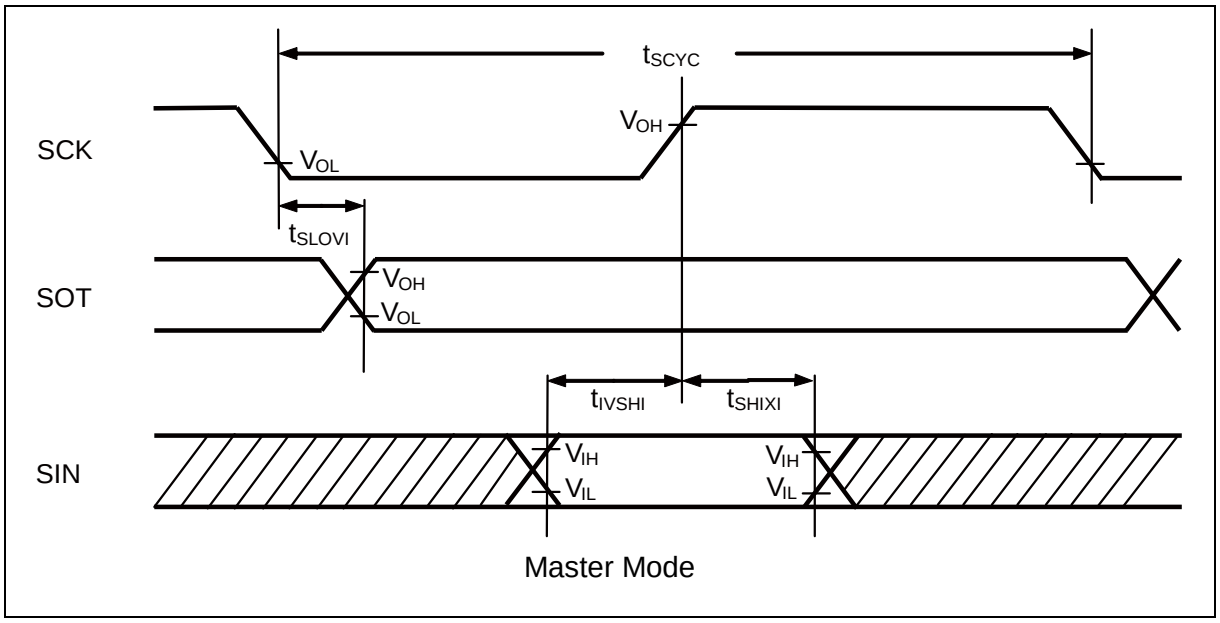
CSIO timing (SMR:MD2-0="010"b)

Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "H" (SMR:SCINV=0)

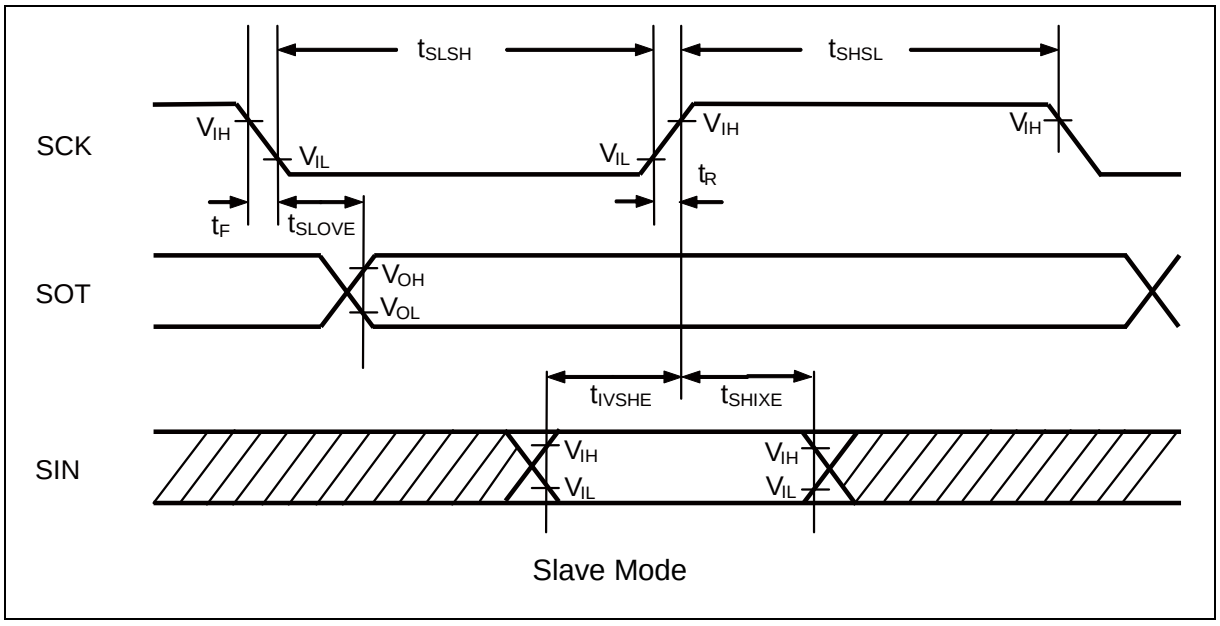
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK3_1,SCK4_1	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK3_1, SCK4_1	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



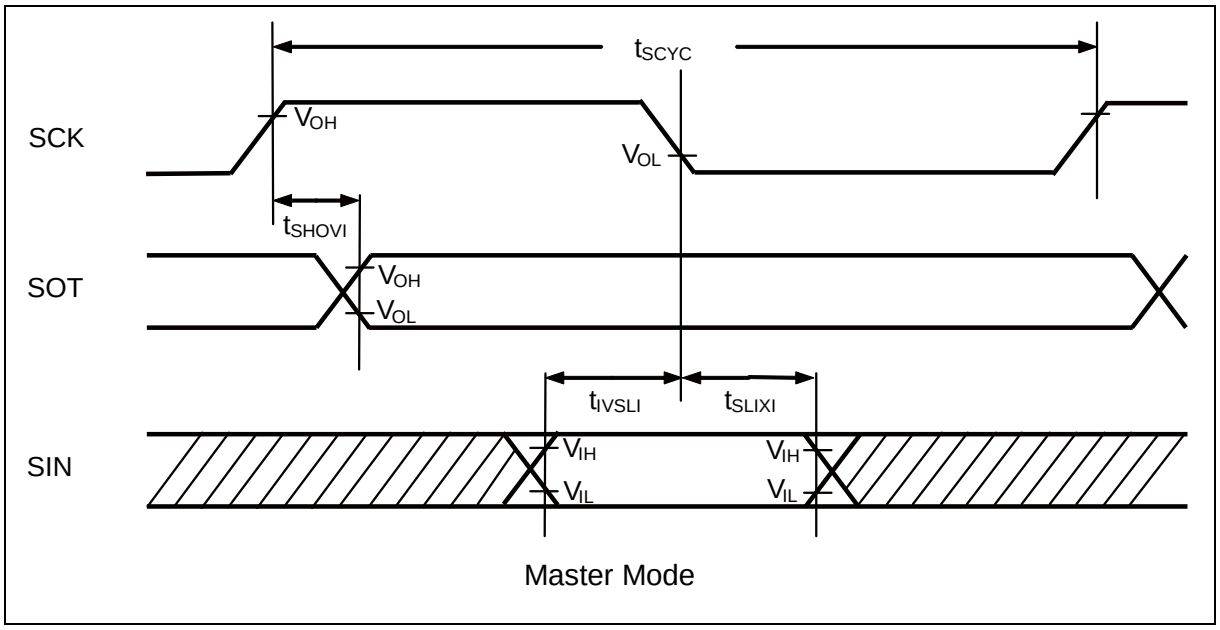
Slave Mode

Normal synchronous transfer (SCR:SPI=0) and serial clock output signal detect level "L"(SMR:SCINV=1)

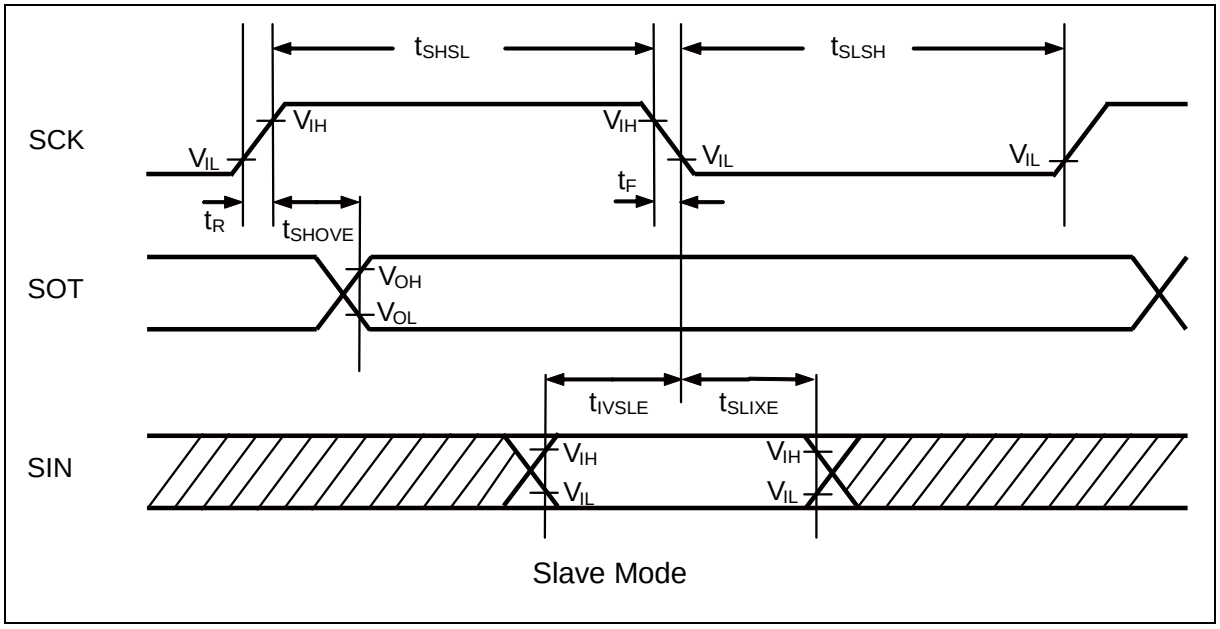
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK3_1,SCK4_1	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK3_1, SCK4_1	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



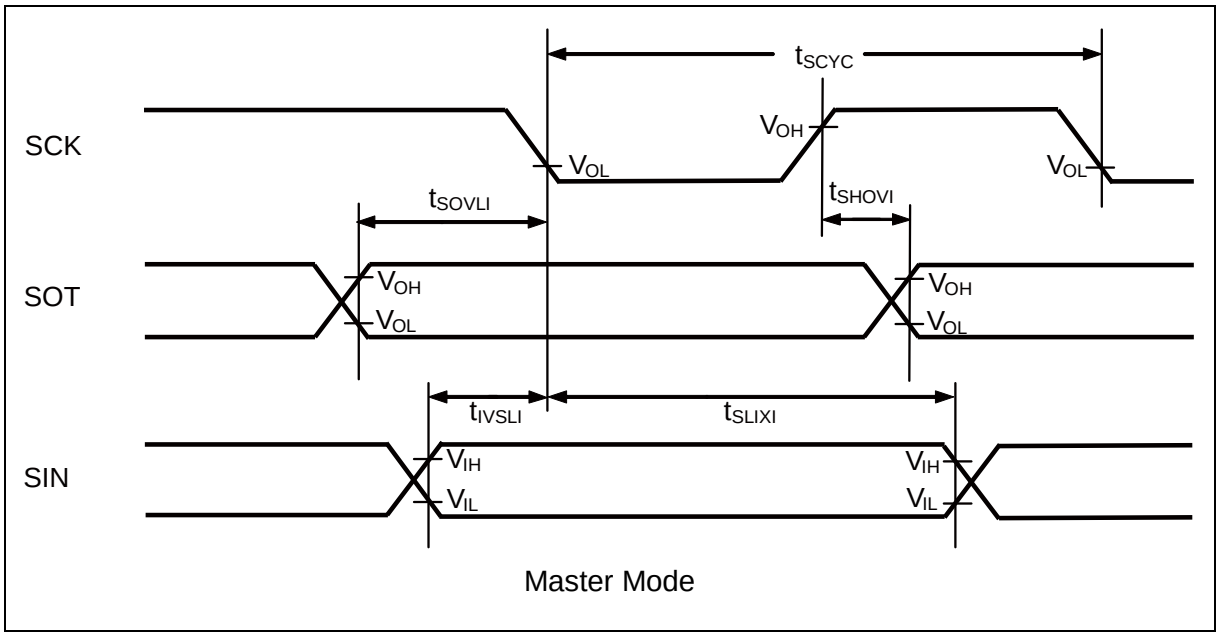
Slave Mode

SPI compatible (SCR:SPI=1) and serial clock output signal detect level "H"(SMR:SCINV=0)

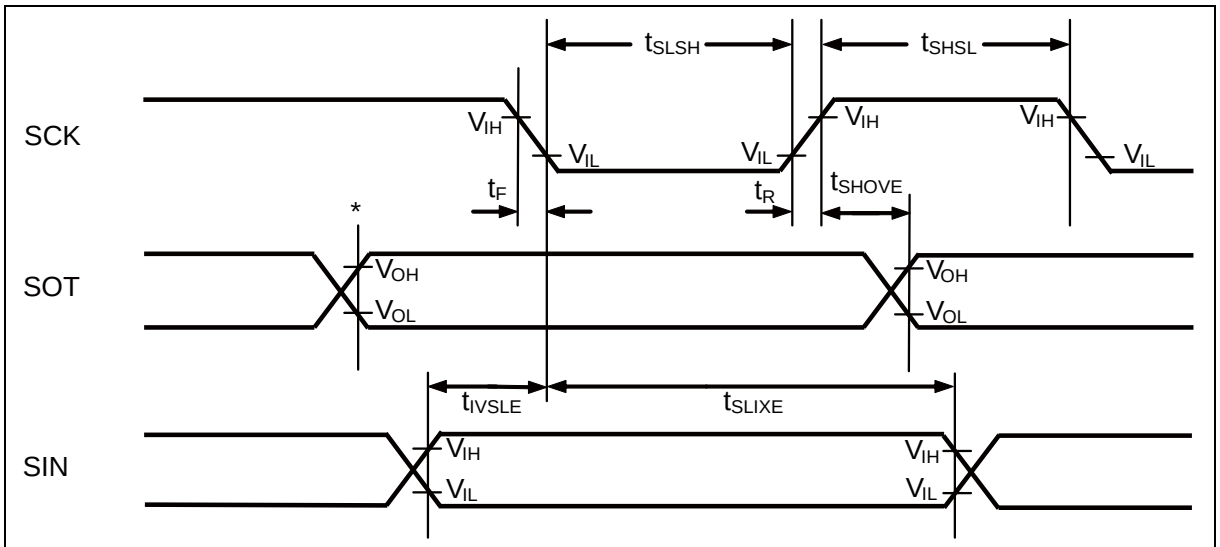
(T_A: Recommended operating conditions, V_{CC} =5.0V±10% , V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK3_1,SCK4_1	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-30	+30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLI}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		30	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT ⇒ SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		$2t_{CPP}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK3_1,SCK4_1	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↑ ⇒ SOT delay time	t_{SHOVE}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	30	ns	
Valid SIN ⇒ SCK ↓ setup time	t_{IVSLE}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		10	-	ns	
SCK ↓ ⇒ Valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK3_1, SCK4_1		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4, SCK3_1,SCK4_1		-	5	ns	

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



*: Changes when writing to TDR register

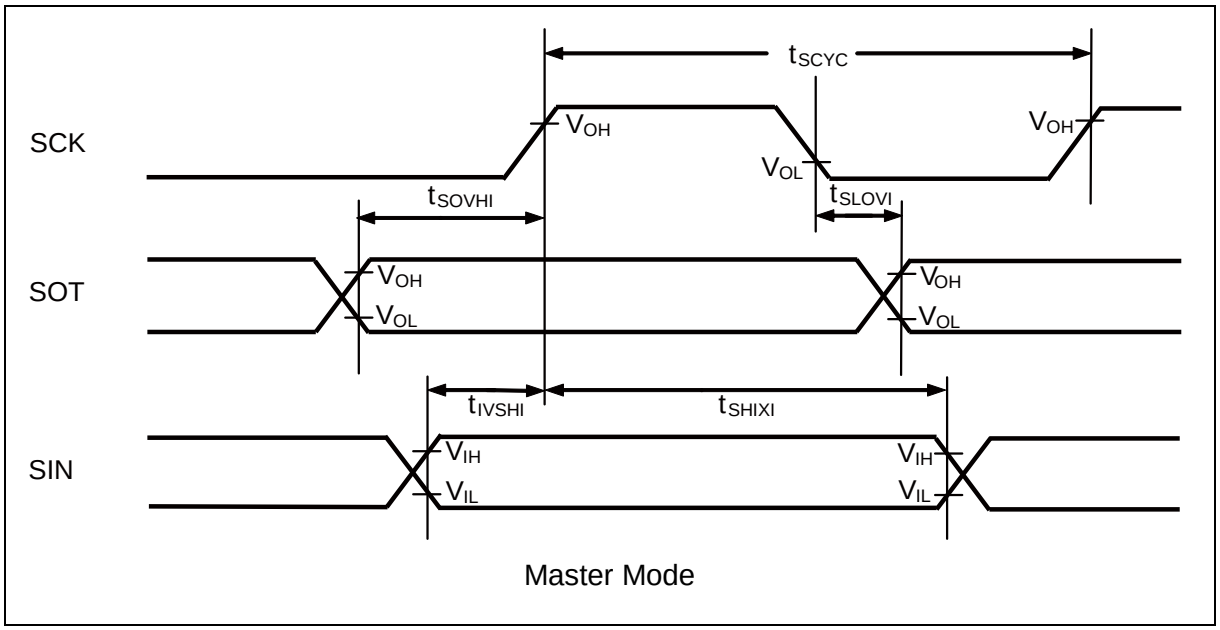
Slave Mode

SPI compatible (SCR:SPI=1) and serial clock output signal detect level "L"(SMR:SCINV=1)

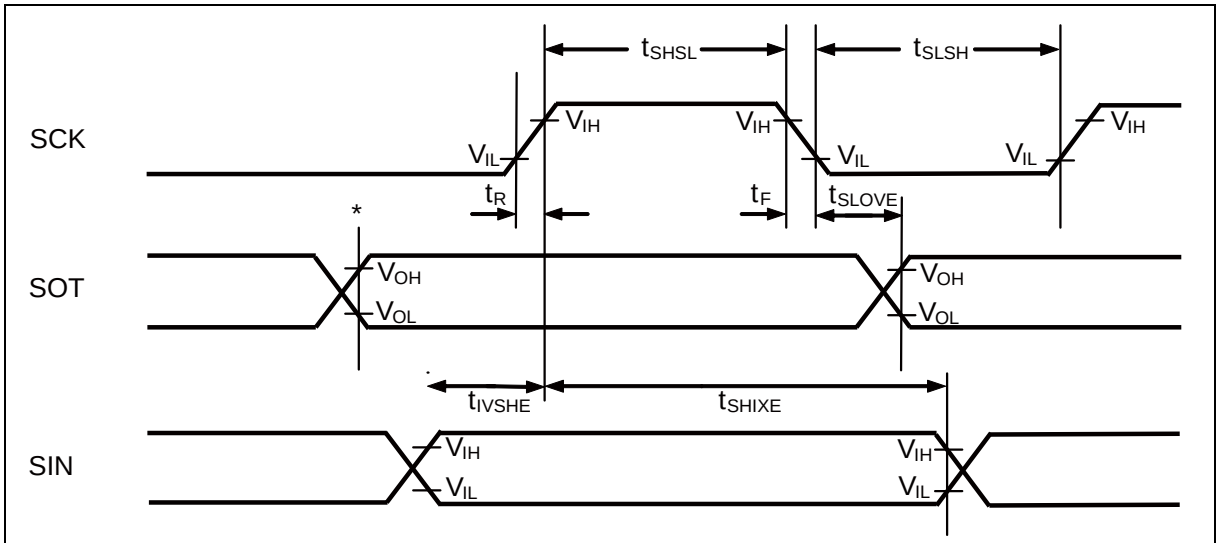
(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4, SCK3_1,SCK4_1	Master mode C_L=50pF	$4t_{CPP}$	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-30	+30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHI}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		30	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT ⇒ SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		$2t_{CPP}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1	Slave mode C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	-	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOVE}	SCK0 to SCK4, SCK3_1,SCK4_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	30	ns	
Valid SIN ⇒ SCK ↑ setup time	t_{IVSHE}	SCK0 to SCK4, SCK3_1, SCK4_1, SIN0 to SIN4, SIN3_1, SIN4_1		10	-	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4, SCK3_1, SCK4_1 SCK0 to SCK4, SCK3_1,SCK4_1		-	5	ns	
SCK rise time	t_R			-	5	ns	

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



*: Changes when writing to TDR register

Slave Mode

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H"(SMR,SCSFR:SCINV=0)
- Serial chip select inactive level "H"(SCSCR,SCSFR:CSLVL=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ ⇒ SCK ↓ setup time	t_{CSSI}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode C_L=50pF	t_{CSSU} *1+0	t_{CSSU} *1+50	ns	
SCK ↑ ⇒ SCS ↑ hold time	t_{CSHI}			t_{CSHD} *2-50	t_{CSHD} *2+0	ns	
SCS deselect time	t_{CSDI}			-50+5t_{CPP} +t_{CSDS} *3	+50+5t_{CPP} +t_{CSDS} *3	ns	
SCS ↓ ⇒ SCK ↓ setup time	t_{CSSE}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↑ ⇒ SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}			3t_{CPP}+30	-	ns	
SCS ↓ ⇒ SOT delay time	t_{DSE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	40	ns	
SCS ↑ ⇒ SOT delay time	t_{DEE}			0	-	ns	

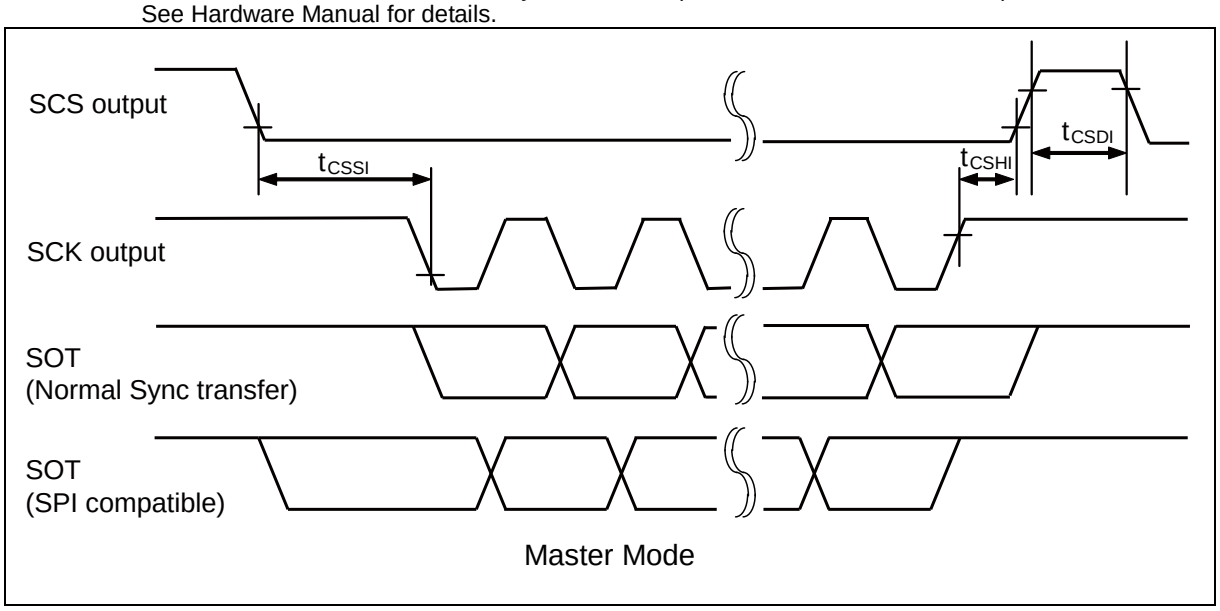
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK ↓ ⇒ SCS ↓ clock switch time	t_{SCC}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode round operation C_L=50pF	$3t_{CPP}$+0	$3t_{CPP}$+50	ns	

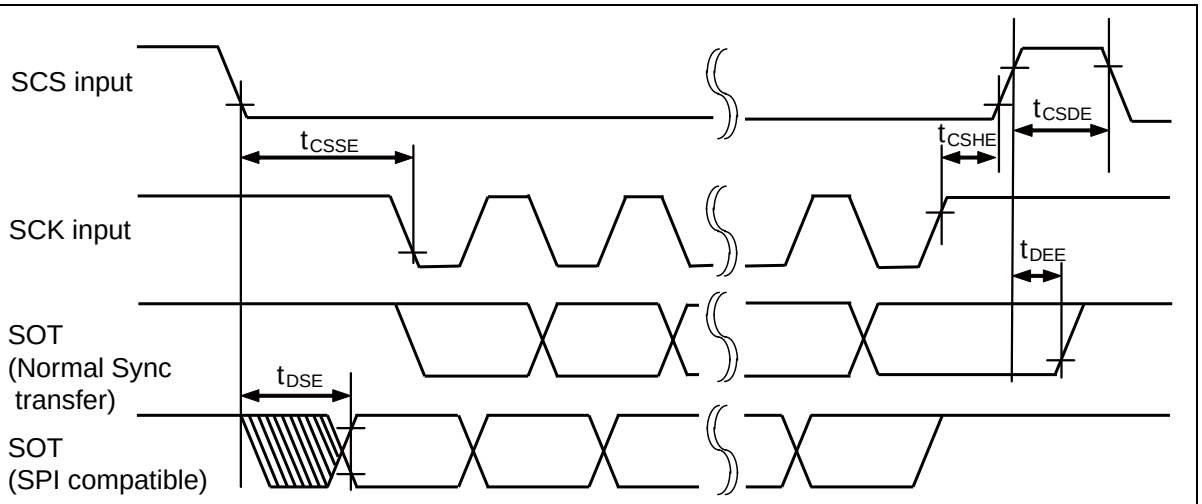
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

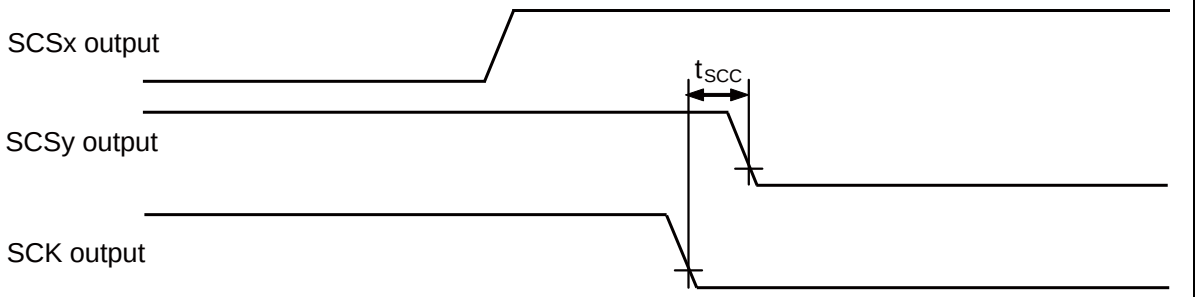
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.





Slave Mode



Clock switching example by master mode round operation (x,y=0,1,2,3)

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L"(SMR,SCSFR:SCINV=1)
- Serial chip select inactive level "H"(SCSCR,SCSFR:CSLVL=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↓ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode C_L=50pF	t_{CSSU} *1+0	t_{CSSU} *1+50	ns	
SCK ↓ ⇒ SCS ↑ hold time	t_{CSHI}			t_{CSHD} *2-50	t_{CSHD} *2+0	ns	
SCS deselect time	t_{CSDI}			-50+5t_{CPP} +t_{CSDS} *3	+50+5t_{CPP} +t_{CSDS} *3	ns	
SCS ↓ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↓ ⇒ SCS ↑ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}			3t_{CPP}+30	-	ns	
SCS ↓ ⇒ SOT delay time	t_{DSE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	40	ns	
SCS ↑ ⇒ SOT delay time	t_{DEE}			0	-	ns	

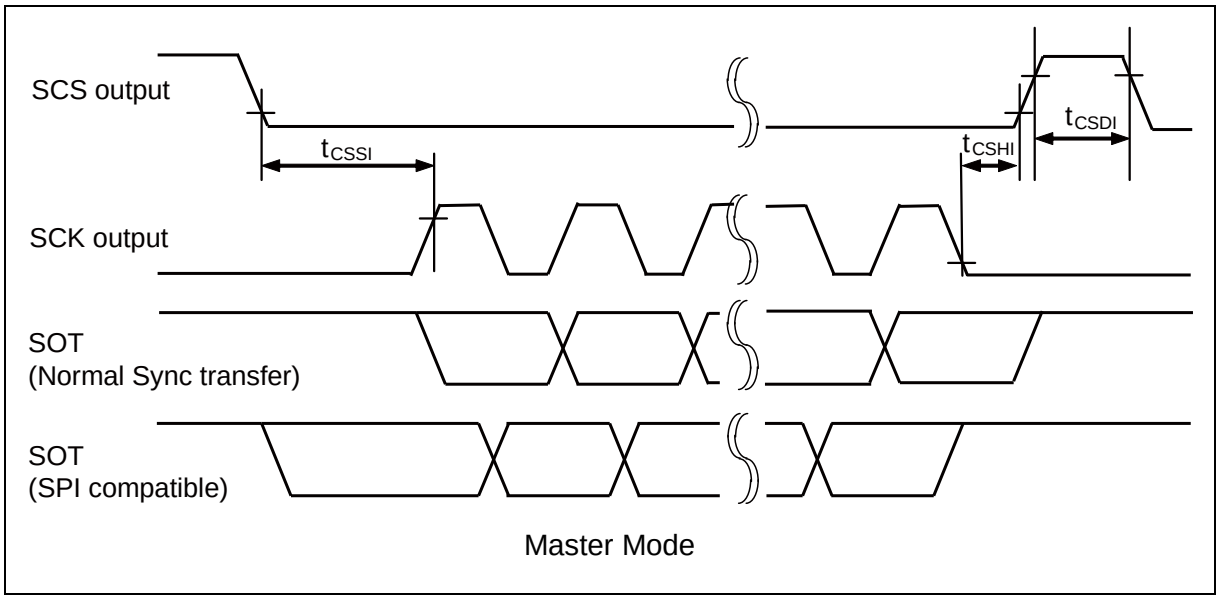
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK ↑ ⇒ SCS ↓ clock switch time	t_{SCC}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode round operation C_L=50pF	$3t_{CPP}$+0	$3t_{CPP}$+50	ns	

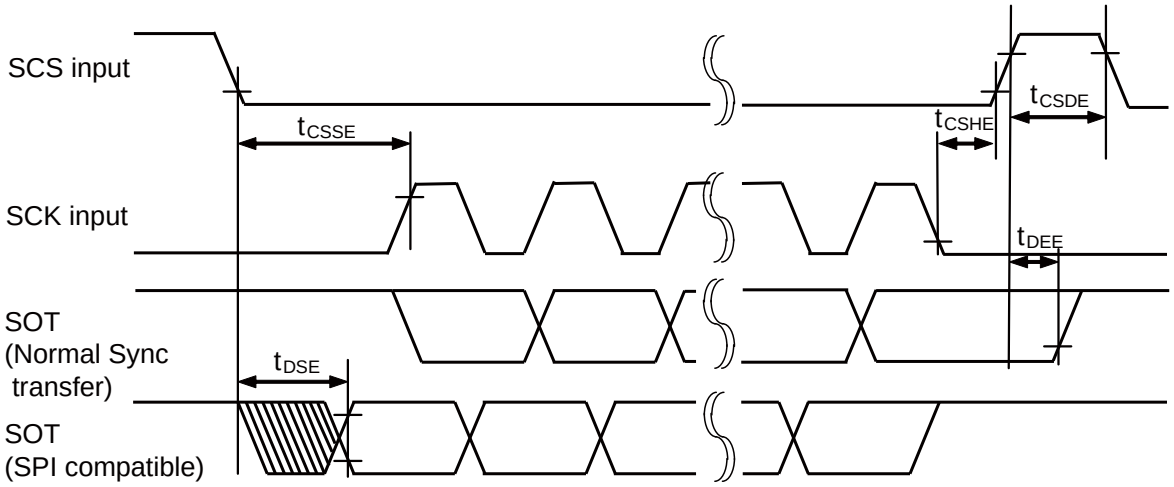
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

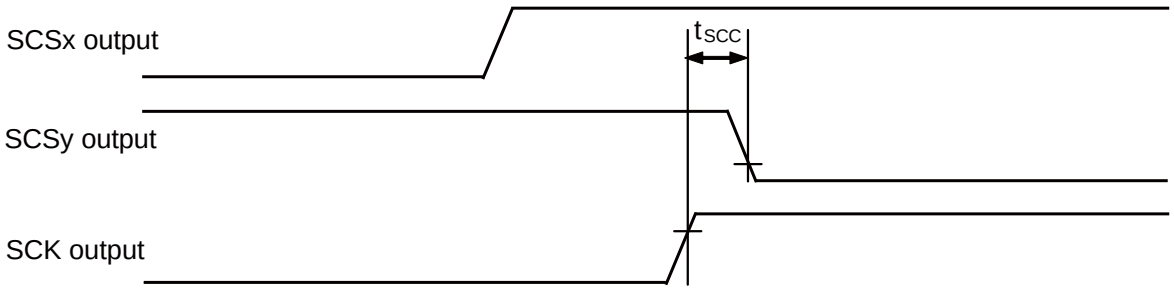
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.





Slave Mode



Clock switching example by master mode round operation (x,y=0,1,2,3)

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "H"(SMR,SCSFR:SCINV=0)
- Serial chip select inactive level "L"(SCSCR,SCSFR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↓ setup time	t_{CSSI}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS0 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode C_L=50pF	t_{CSSU} *1+0	t_{CSSU} *1+50	ns	
SCK ↑ ⇒ SCS ↓ hold time	t_{CSHI}			t_{CSHD} *2-50	t_{CSHD} *2+0	ns	
SCS deselect time	t_{CSDI}			-50+5t_{CPP} +t_{CSDS} *3	+50+5t_{CPP} +t_{CSDS} *3	ns	
SCS ↑ ⇒ SCK ↓ setup time	t_{CSSE}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS0 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↑ ⇒ SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}			3t_{CPP}+30	-	ns	
SCS ↑ ⇒ SOT delay time	t_{DSE}	SCS0 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	40	ns	
SCS ↓ ⇒ SOT delay time	t_{DEE}			0	-	ns	

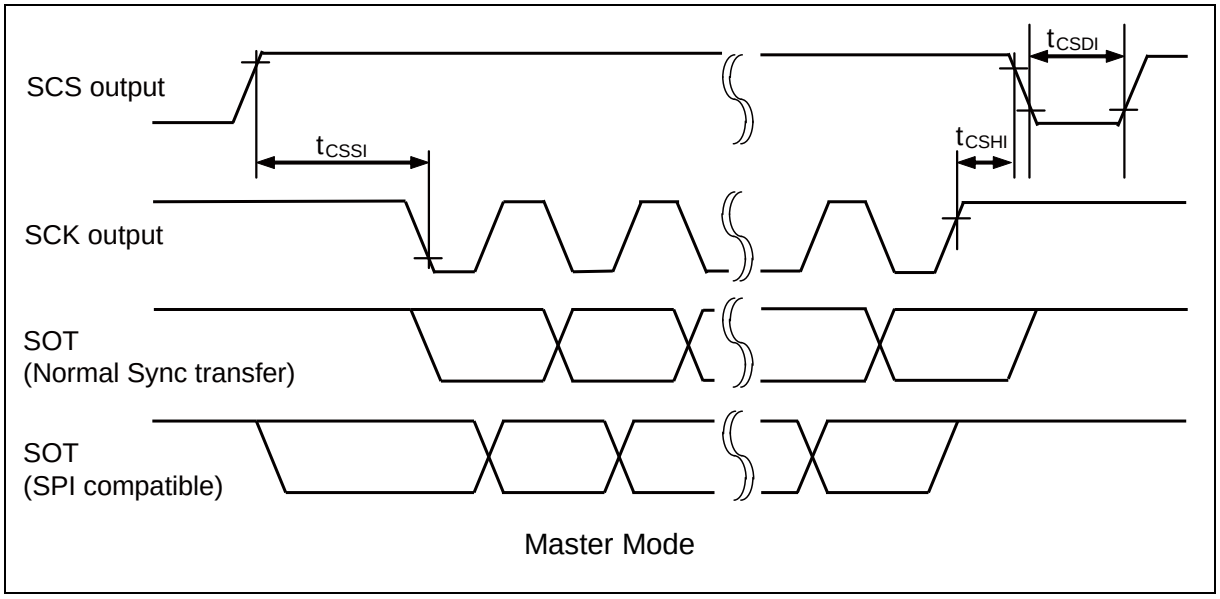
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK ↓ ⇒ SCS ↑ clock switch time	t_{SCC}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS0 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode round operation C_L=50pF	$3t_{CPP}$+0	$3t_{CPP}$+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

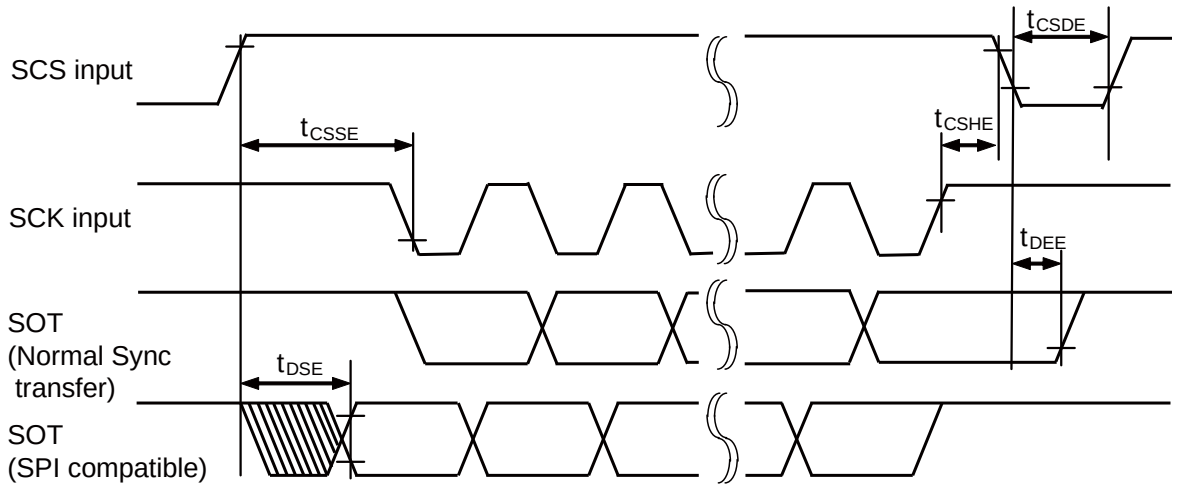
*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock
For details of *1, *2 and *3 above, see Hardware Manual.

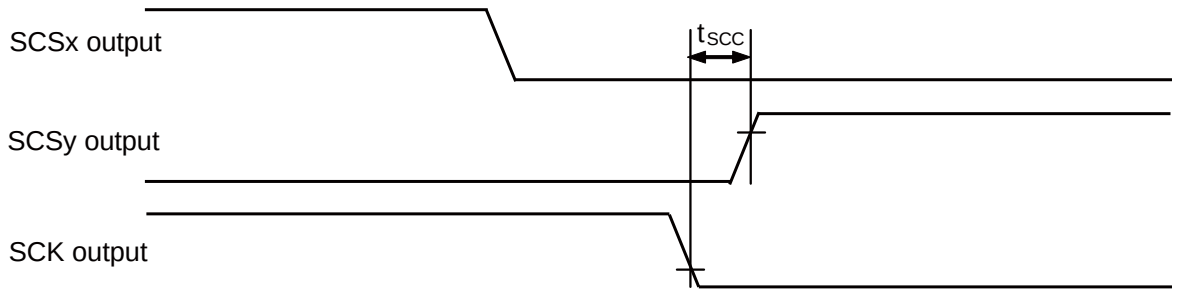
Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master Mode



Slave Mode



Clock switching example by master mode round operation (x,y=0,1,2,3)

When the serial chip select is used (SCSCR:CSEN=1)

- Serial clock output signal detect level "L"(SMR,SCSFR:SCINV=1)
- Serial chip select inactive level "L"(SCSCR,SCSFR:CSLVL=0)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSI}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode C_L=50pF	t_{CSSU} *1+0	t_{CSSU} *1+50	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHI}			t_{CSHD} *2-50	t_{CSHD} *2+0	ns	
SCS deselect time	t_{CSDI}			-50+5t_{CPP} +t_{CSDS} *3	+50+5t_{CPP} +t_{CSDS} *3	ns	
SCS ↑ ⇒ SCK ↑ setup time	t_{CSSE}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Slave mode C_L=50pF	3t_{CPP}+30	-	ns	
SCK ↓ ⇒ SCS ↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}			3t_{CPP}+30	-	ns	
SCS ↑ ⇒ SOT delay time	t_{DSE}	SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1, SOT0 to SOT4, SOT3_1,SOT4_1		-	40	ns	
SCS ↓ ⇒ SOT delay time	t_{DEE}			0	-	ns	

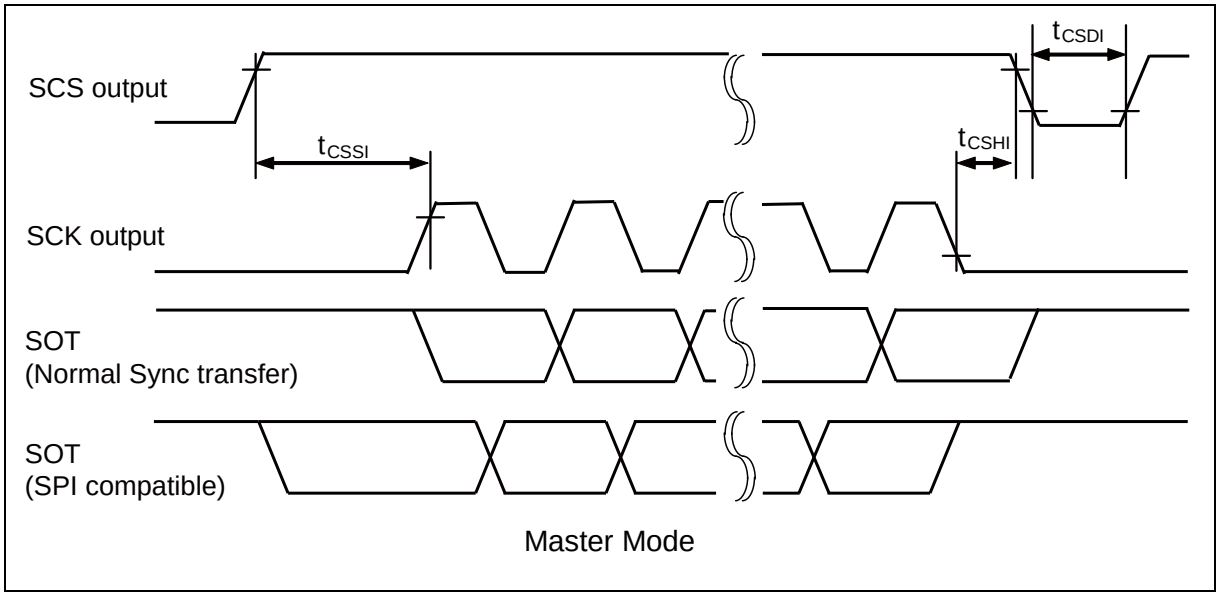
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCK ↑ ⇒ SCS ↑ clock switch time	t_{SCC}	SCK1 to SCK4, SCK3_1,SCK4_1, SCS1 to SCS3, SCS3_1, SCS40 to SCS43 SCS40_1 to SCS43_1	Master mode round operation C_L=50pF	$3t_{CPP}$+0	$3t_{CPP}$+50	ns	

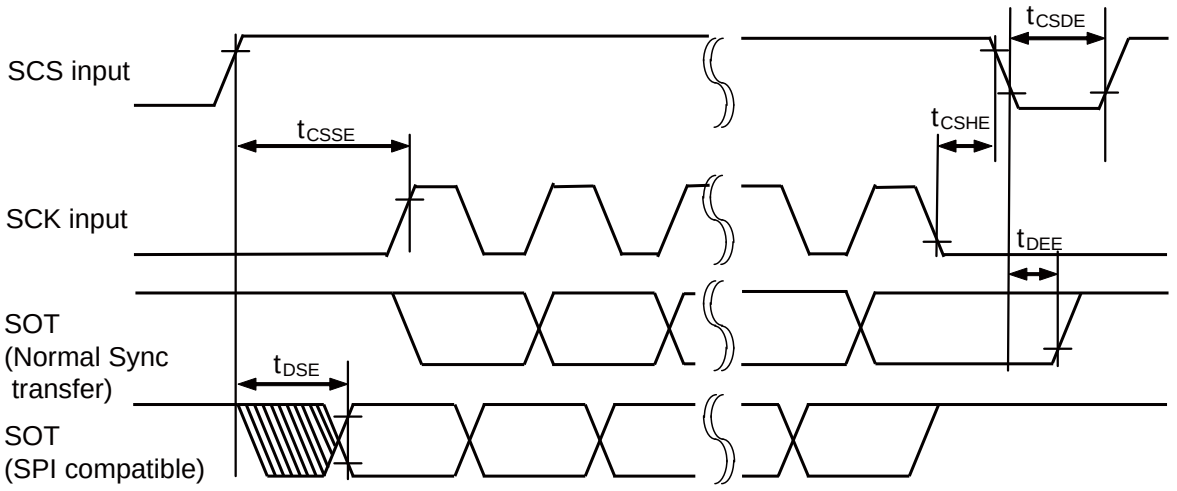
*1: t_{CSSU} =SCSTR:CSSU7-0 × Serial chip select timing operation clock

*2: t_{CSHD}=SCSTR:CSHD7-0 × Serial chip select timing operation clock

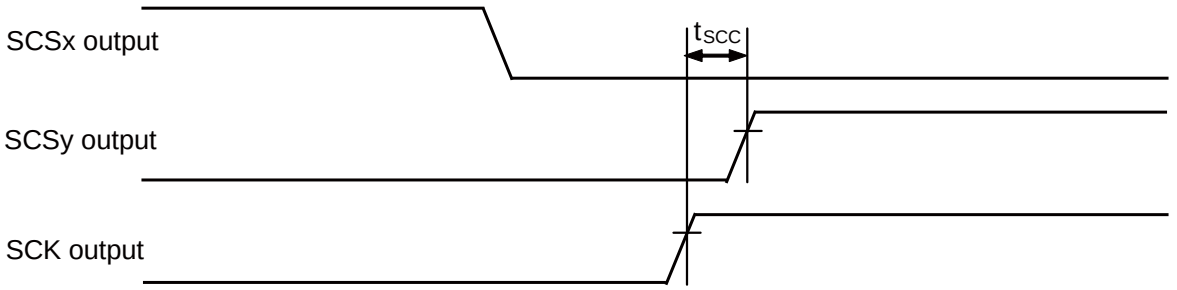
*3: t_{CSDS}=SCSTR:CSDS15-0 × Serial chip select timing operation clock
For details of *1, *2 and *3 above, see Hardware Manual.

Notes:
- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.





Slave Mode

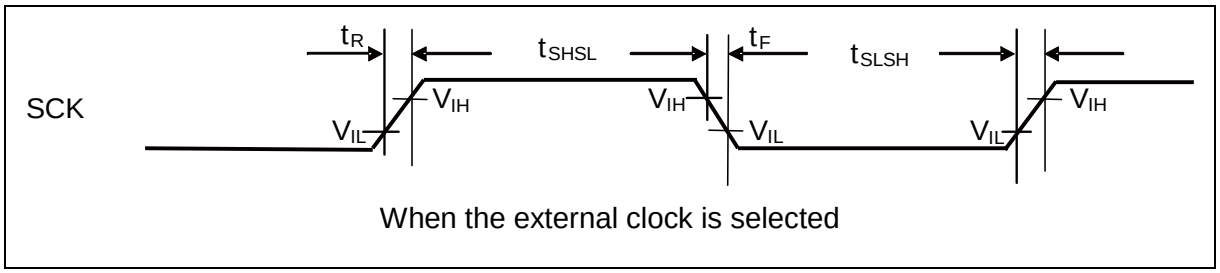


Clock switching example by master mode round operation (x,y=0,1,2,3)

UART (Async Serial Interface) timing (SMR:MD2-0="000"b, "001"b)
When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK3_1,SCK4_1	C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	

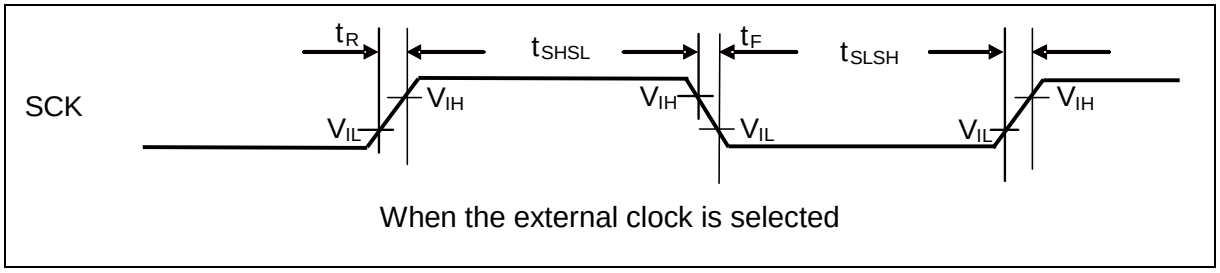


When the external clock is selected

LIN interface (v2.1) (LIN Communication Control Interface (v2.1)) timing (SMR:MD2-0="011"b)
When the external clock is selected (BGR:EXT=1)

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK4, SCK3_1,SCK4_1	C_L=50pF	t_{CPP}+10	-	ns	
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When the external clock is selected

I^2C timing (SMR:MD2-0="100"b)

(T_A: Recommended operating conditions, V_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

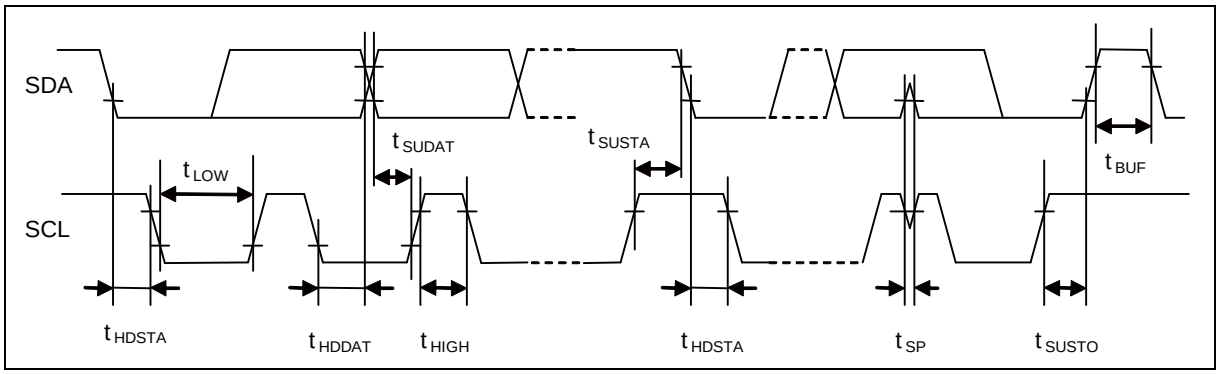
Parameter	Symbol	Pin name	Conditions	Standard mode		High-speed mode*3		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL)	C_L=50pF R=(V_P/I_{OL}) *1	0	100	0	400	kHz	
"Repeat START condition" hold time SDA ↓ → SCL ↓	t_{HDSTA}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL) SOT0,SOT1, SOT3,SOT4, SOT3_1,SOT4_1 (SDA)		4.0	-	0.6	-	µs	
"L" width for SCL clock	t_{LOW}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL)		4.7	-	1.3	-	µs	
"H" width for SCL clock	t_{HIGH}			4.0	-	0.6	-	µs	
"Repeat START condition" setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0,SCK1, SCK3,SCK4, SCK3_1,SCK4_1 (SCL) SOT0,SOT1, SOT3,SOT4, SOT3_1,SOT4_1 (SDA)		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}			0	3.45 *2	0	0.90 *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}			250	-	100	-	ns	
"STOP condition" setup time SCL ↑ → SDA ↑	t_{SUSTO}			4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}	-		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	-		$2t_{CPP}$ *4	-	$2t_{CPP}$ *4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. V_P shows that the power supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "$t_{SUDAT} \geq 250$ ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the peripheral bus to 8MHz or more when use I^2C.

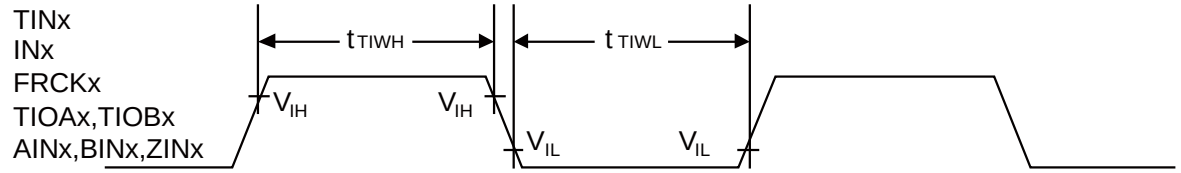


12.4.5 Timer input timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN3, IN0 to IN7, FRCK0 to FRCK5, TIOA0, TIOA1, TIOB0, TIOB1	-	$4t_{CPP}$	-	ns	
		AIN0,AIN1, BIN0,BIN1, ZIN0,ZIN1	-	$2t_{CPP}$	-	ns	

Timer input timing

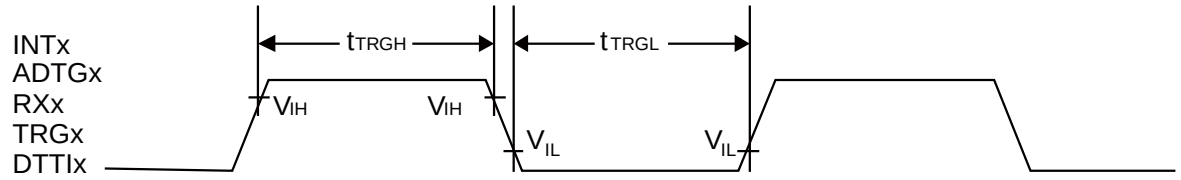


12.4.6 Trigger input timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10% V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT7, ADTG0 to ADTG2, RX0 to RX2, TRG0 to TRG5, DTTI0,DTTI1	-	$5t_{CPP}$	-	ns	
				1	-	µs	At Stop mode

Trigger input timing

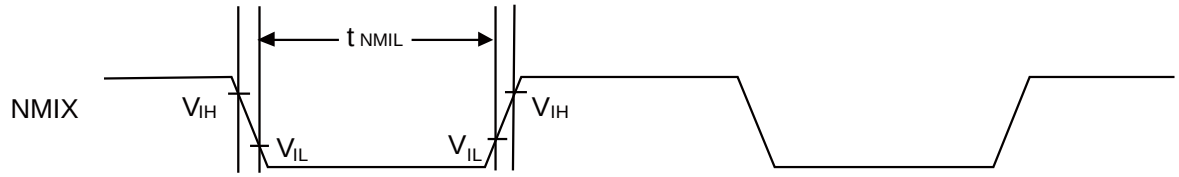


12.4.7 NMI input timing

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	-	$4t_{CPP}$	-	ns	

NMIX input timing



12.4.8 Low-voltage detection (External low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{DP5}	VCC5	-	-	-	5.5	V	
Detection voltage	V_{DL}	VCC5	*1	3.7	3.9	4.1	V	When power supply voltage falls and detection level is set initially
Hysteresis width	V_{HYS}	VCC5	-	-	-	125	mV	When power supply voltage rises
Low-voltage detection time	Td	-	-	-	-	30	µs	
Power supply voltage fluctuation rate	-	VCC5	-	-2	-	2	V/ms	*2

*1: If the fluctuation of the power supply has exceeded the detection voltage range within the time less than the low-voltage detection time (Td), there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply within the limits of the power supply voltage fluctuation rate.

12.4.9 Low-voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

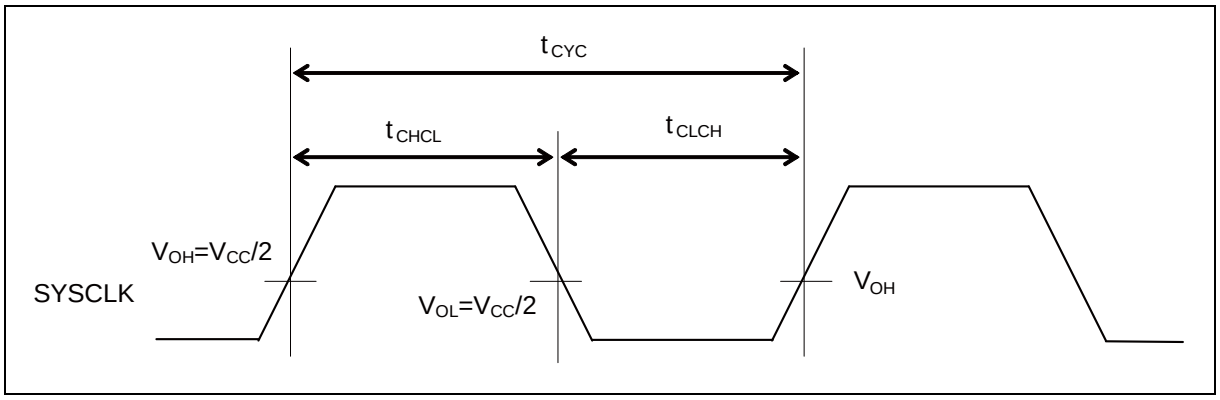
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	-	-	-	-	1.3	V	
Detection voltage	V_{RDL}	-	*	0.8	0.9	1.0	V	When power supply voltage falls
Hysteresis width	V_{RHYS}	-	-	-	-	50	mV	When power supply voltage rises
Low-voltage detection time	-	-	-	-	-	30	µs	

*: If the fluctuation of the power supply is faster than the low-voltage detection time (Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

12.4.10 Clock output timing

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	SYSCLK	-	t_{CPT}	-	ns	
SYSCLK ↑ → SYSCLK ↓	t_{CHCL}	SYSCLK		(1/2 t_{CYC})- 7	(1/2 t_{CYC})+ 7	ns	
SYSCLK ↓ → SYSCLK ↑	t_{CLCH}	SYSCLK		(1/2 t_{CYC})- 7	(1/2 t_{CYC})+ 7	ns	



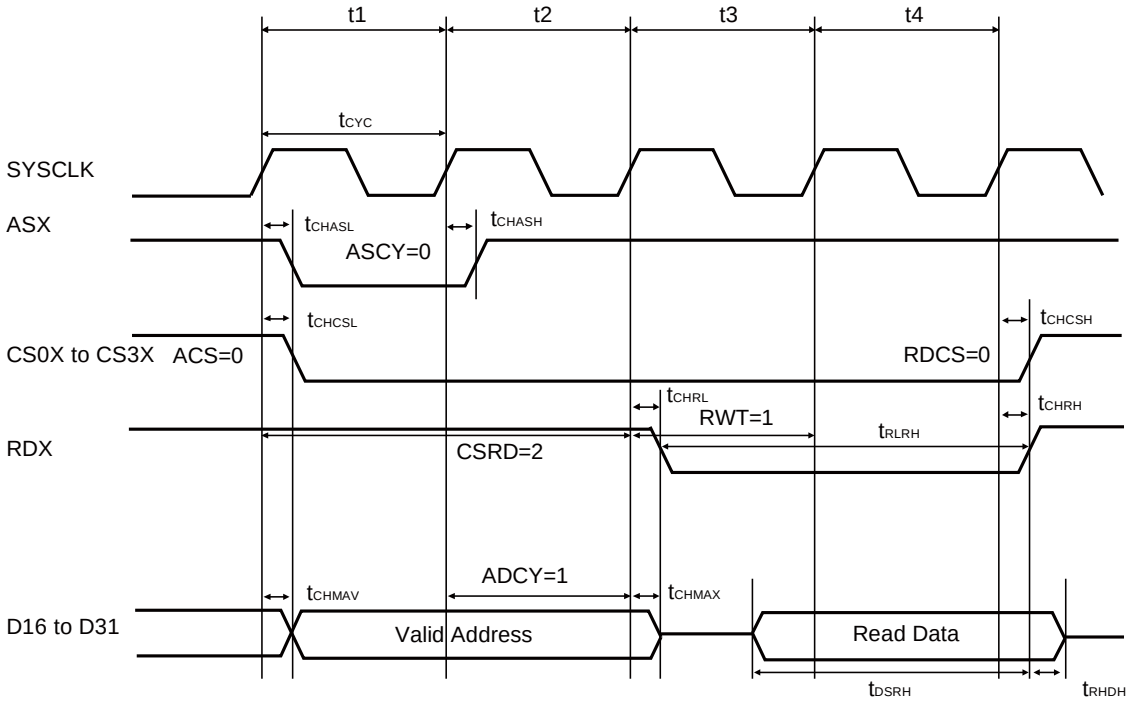
12.4.11 External bus I/F (synchronous mode) timing

(T_A: Recommended operating conditions, V_{CC} =AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)
(External load capacitance 50pF)

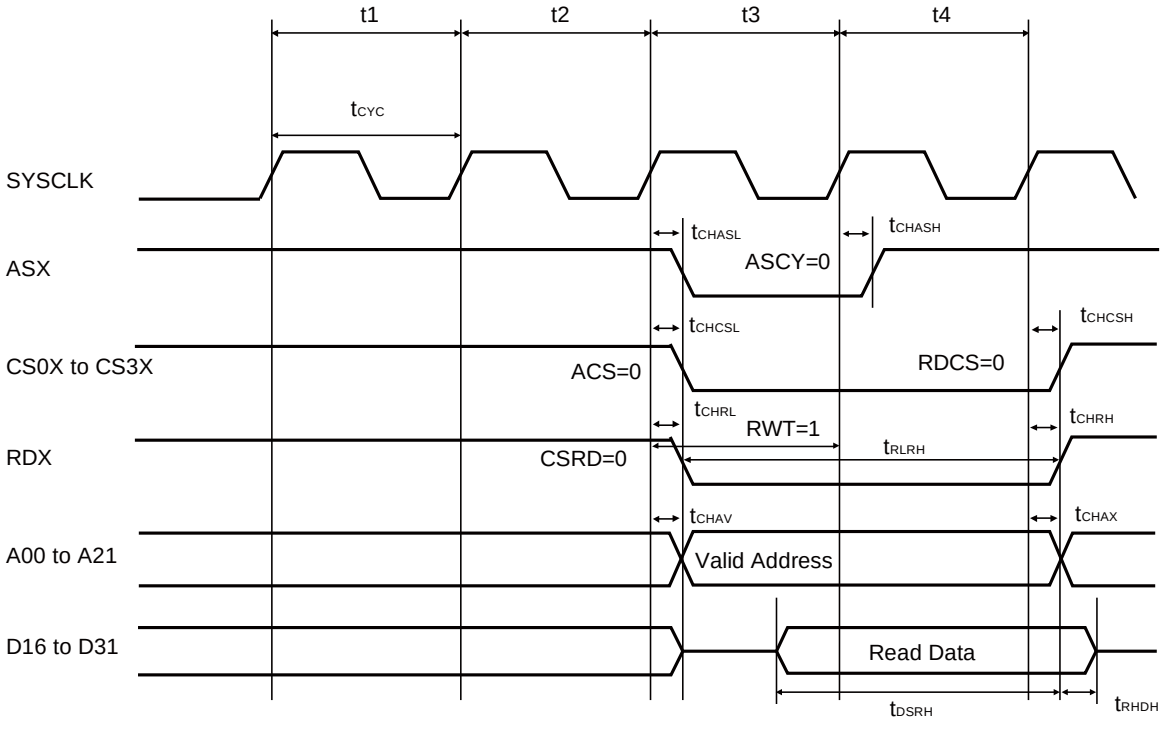
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	
ASX delay time	t_{CHASL}, t_{CHASH}	SYSCLK, ASX	0.5	18.0	ns	
CS0X to CS3X delay time	t_{CHCSL}, t_{CHCSH}	SYSCLK, CS0X to CS3X	0.5	18.0	ns	
A00 to A21 delay time	t_{CHAV}, t_{CHAX}	SYSCLK, A00 to A21	0.5	18.0	ns	
RDX delay time	t_{CHRL}, t_{CHRH}	SYSCLK, RDX	0.5	18.0	ns	
RDX minimum pulse	t_{RLRH}	RDX	t_{CYC} × 2 - 20	-	ns	RWT=1, set RWT to 1 or more. *
Data setup → RDX ↑ time	t_{DSRH}	RDX, D16 to D31	18 + t_{CYC}	-	ns	RWT=1, set RWT to 1 or more. *
RDX ↑ → data hold	t_{RHDH}		0	-	ns	
WRnX delay time	t_{CHWL}, t_{CHWH}	SYSCLK, WR0X, WR1X	0.5	18.0	ns	
WRnX minimum pulse width	t_{WLWH}	WR0X, WR1X	t_{CYC} - 10	-	ns	WWT=0*
SYSCLK ↑ → data output time	t_{CHDV}	SYSCLK, D16 to D31	0.5	18.0	ns	
SYSCLK ↑ → data hold time	t_{CHDX}		-	18	ns	Set WRCS to 1 or more.
SYSCLK ↑ → address output time	t_{CHMAV}	SYSCLK, D16 to D31	0.5	18.0	ns	
SYSCLK ↑ → address hold time	t_{CHMAX}		-	18	ns	In multiplex mode, set as follows: Set CSWR and CSRD to 2 or more. Set to ADCY>ASCY. To prevent protocol violation, satisfy the following conditions: ADCY + 1 ≤ ACS + CSRD ADCY + 1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR For details, see Hardware Manual.

*: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

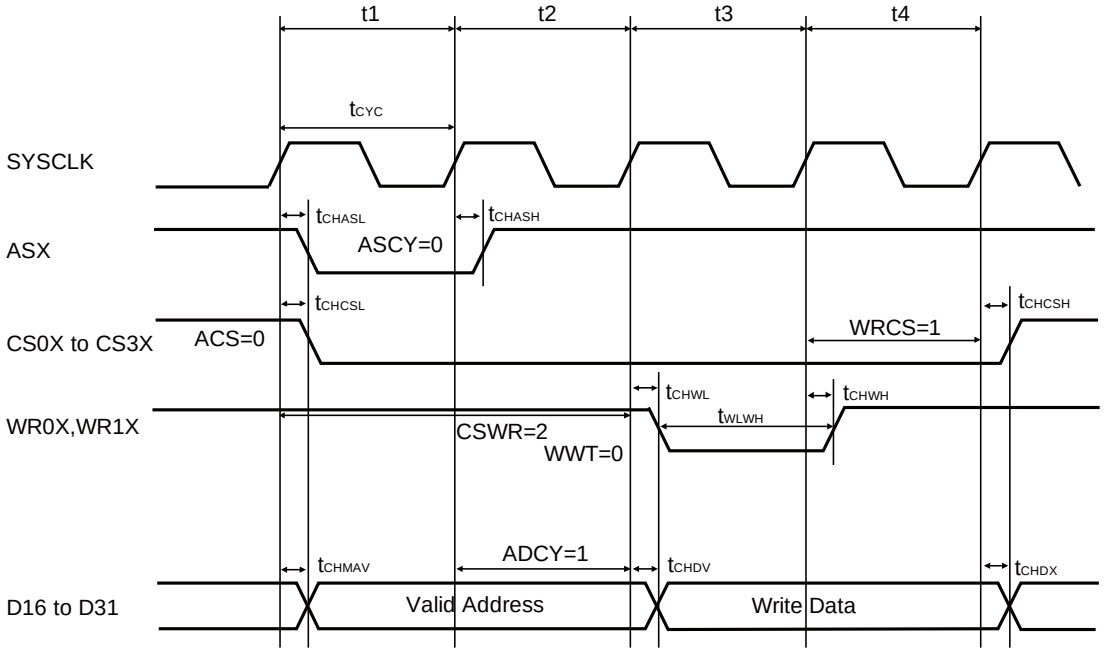
External bus I/F (synchronous mode, read operation, and multiplex mode) timing



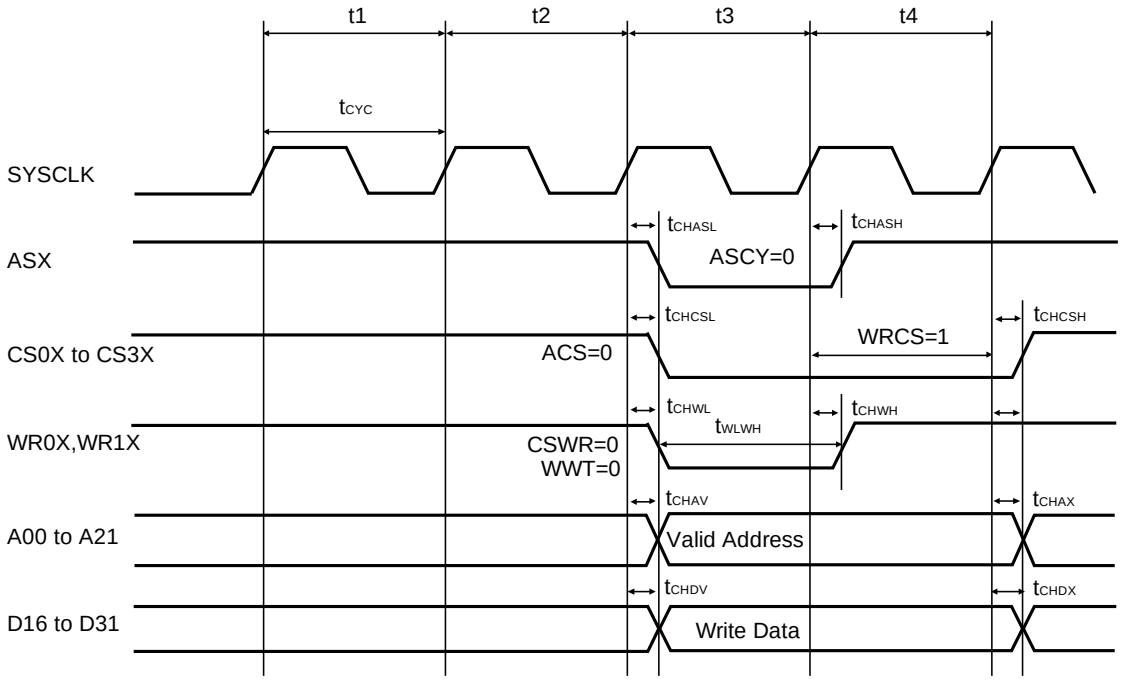
External bus I/F (synchronous mode, read operation, and split mode) timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



External bus I/F (synchronous mode, write operation, and split mode) timing



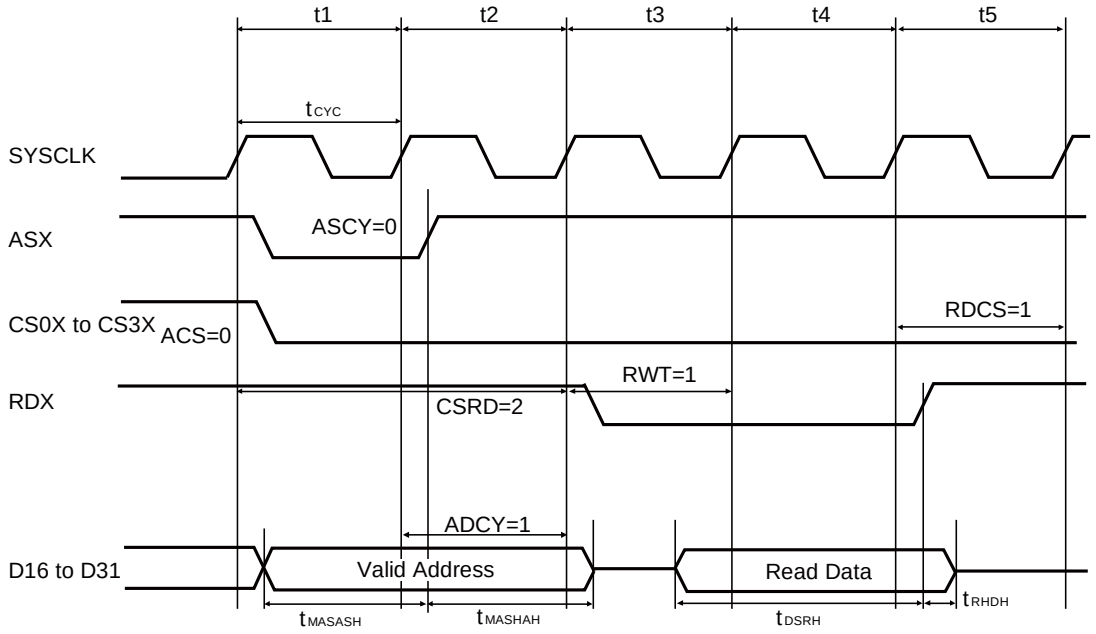
12.4.12 External bus I/F (Asynchronous mode) timing

(T_A: Recommended operating conditions, V_{CC} = AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)
(External load capacitance 50pF)

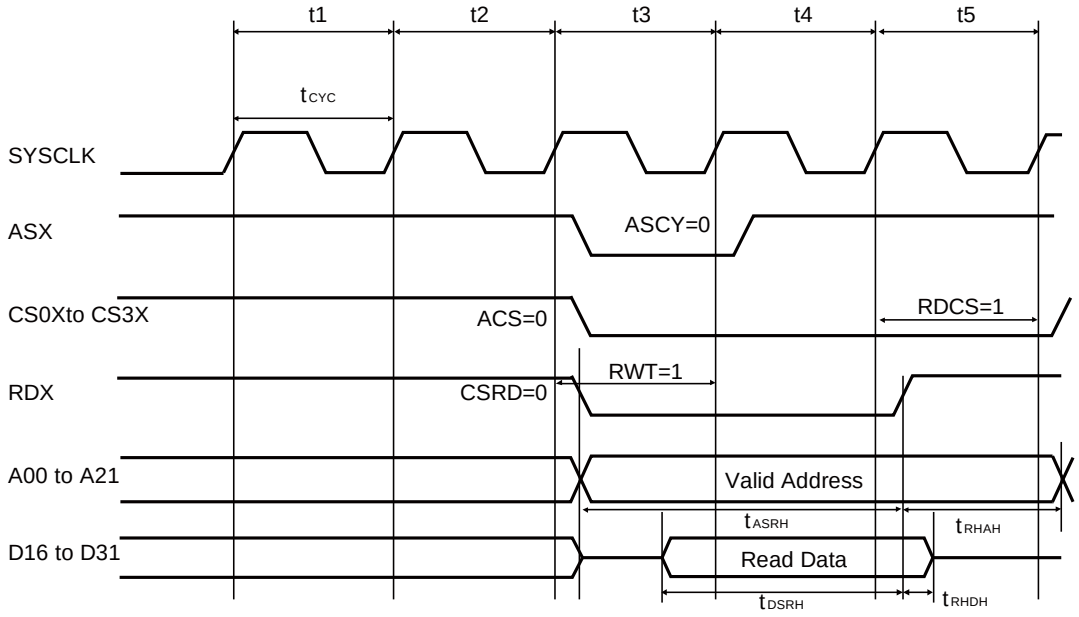
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	25	-	ns	
Address setup → RDX ↑ time	t_{ASRH}	RDX, A00 to A21	2 × t_{CYC} – 12	2 × t_{CYC} + 12	ns	RWT=1, set RWT to 1 or more.*
RDX ↑ → Address hold	t_{RHAH}		t_{CYC} – 12	t_{CYC} + 12	ns	Set RDCS to 1 or more.
Data setup → RDX ↑ time	t_{DSRH}	RDX, D16 to D31	18 +t_{CYC}	-	ns	RWT=1, set RWT to 1 or more.
RDX ↑ → Data hold	t_{RHDH}		0	-	ns	
Address setup → WRnX ↑ time	t_{ASWH}	WR0X to WR1X, A00 to A21	t_{CYC} – 12	t_{CYC} + 12	ns	WWT=0.*
WRnX ↑ → Address hold	t_{WHAH}		t_{CYC} – 12	t_{CYC} + 12	ns	Set WRCS to 1 or more.
Data setup → WRnX ↑ time	t_{DSWH}	WR0X to WR1X, D16 to D31	t_{CYC} – 16	t_{CYC} + 16	ns	WWT=0.*
WRnX ↑ → Data hold	t_{WHDH}		t_{CYC} – 16	t_{CYC} + 16	ns	Set WRCS to 1 or more.
Address setup → ASX ↑ time	t_{MASASH}	ASX, D16 to D31	t_{CYC} – 16	t_{CYC} + 16	ns	ASCY=0.
ASX ↑ → Address hold	t_{MASHAH}		t_{CYC} – 16	t_{CYC} + 16	ns	In multiplex mode, set as follows: Set CSWR and CSRD to 2 or more. Set to ADCY>ASCY. To prevent protocol violation, satisfy the following conditions: ADCY + 1 ≤ ACS + CSRD ADCY + 1 ≤ ACS + CSWR ASCY + 1 ≤ ACS + CSRD ASCY + 1 ≤ ACS + CSWR For details, see Hardware Manual.

*: If the bus is expanded by automatic wait insertion or RDY input, add time (t_{CYC} × the number of expanded cycles) to the rated value.

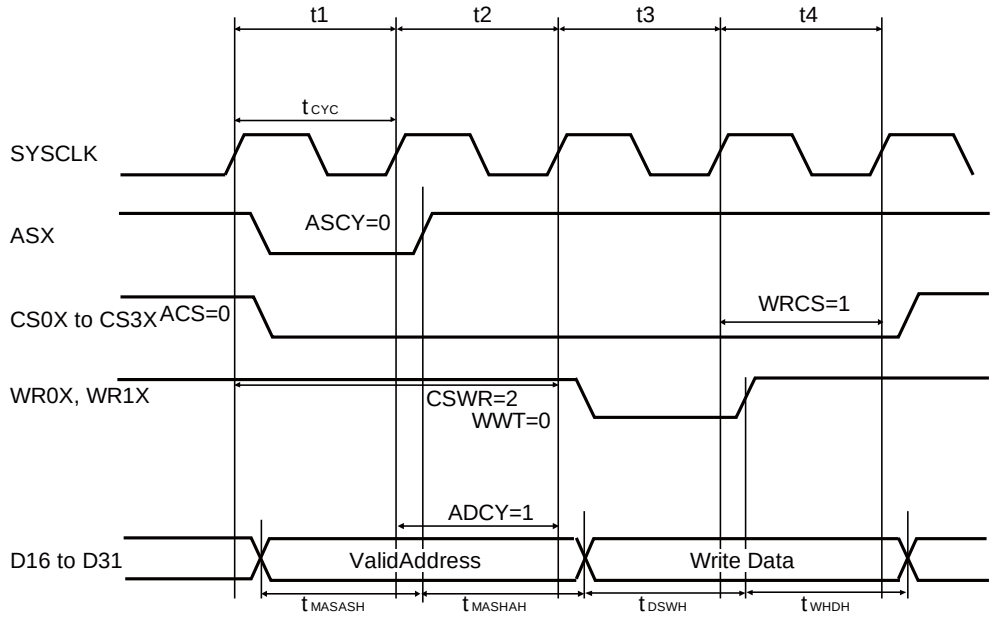
External bus I/F (asynchronous mode, read operation, and multiplex mode) timing



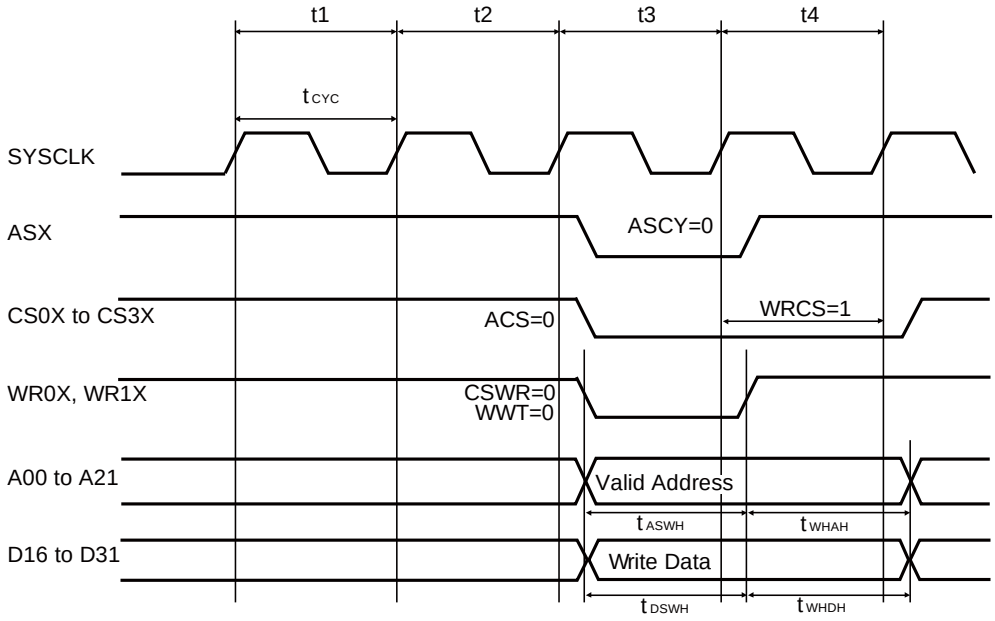
External bus I/F (asynchronous mode, read operation, and split mode) timing



External bus I/F (asynchronous mode, write operation, and multiplex mode) timing



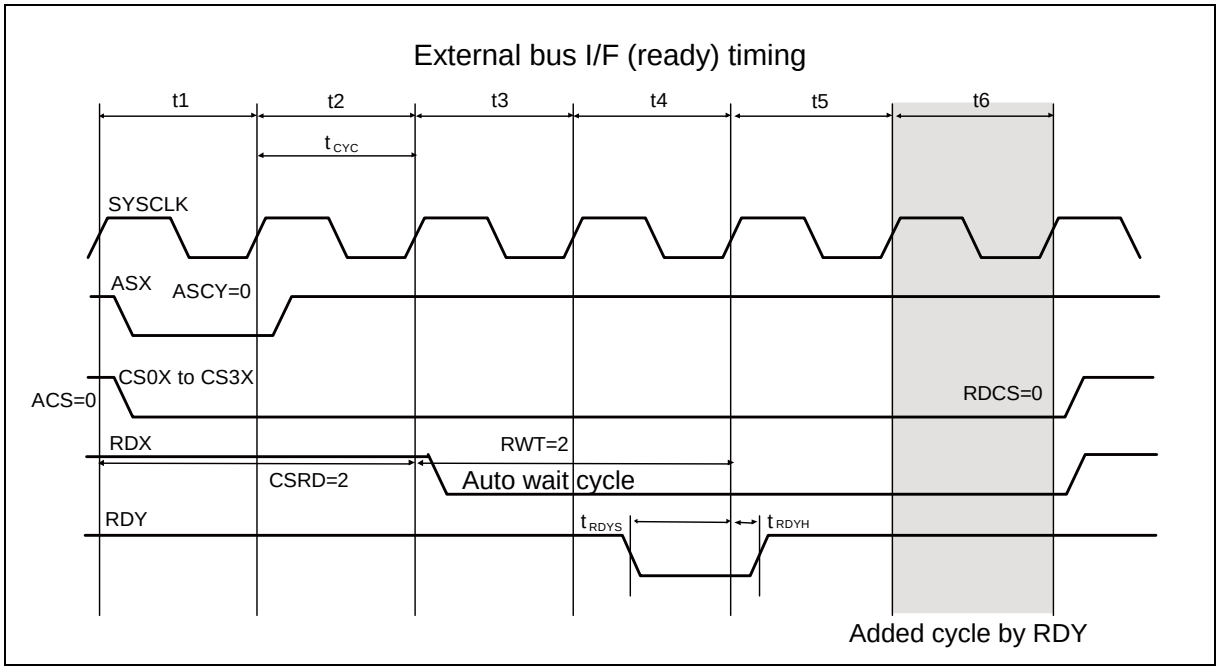
External bus I/F (asynchronous mode, write operation, and split mode) timing



12.4.13 External bus I/F (ready) timing

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)
(External load capacitance 50pF)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Cycle time	t_{CYC}	SYSCLK	50	-	ns	If using RDY, set SYSCLK to 20 MHz or less.
RDY setup time → SYSCLK ↑	t_{RDYS}	SYSCLK, RDY	28	-	ns	
SYSCLK ↑ → RDY hold time	t_{RDYH}	SYSCLK, RDY	0	-	ns	



12.5 A/D Converter

12.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} =5.0V±10%, AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Non linearity error	-	-	-4.0	-	+4.0	LSB	
Differential linearity error	-	-	-1.9	-	+1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN23	AVRL+ 0.5LSB-20	-	AVRL+ 0.5LSB+20	mV	1LSB= (VFST-VOT)/ 4094
Full-scale transition voltage	V_{FST}	AN0 to AN23	AVRH- 1.5LSB-20	-	AVRH- 1.5LSB+20	mV	
Sampling time	t_{SMP}	-	0.3	-	12	µs	*1
Compare time	t_{CMP}	-	0.7	-	28	µs	*1
A/D conversion time	t_{CNV}	-	1.0	-	40	µs	*1
Analog port input current	I_{AIN}	AN0 to AN23	-1.0	-	1.0	µA	$V_{AVSS} \leq V_{AIN} \leq V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN23	AV_{SS}	-	AVRH	V	
Reference voltage	AVRH	AVRH1, AVRH2, AVRH3	4.5	-	5.5	V	Avcc ≥AVRH
	AVRL	AVRL1, AVRL2, AVRL3	-	0.0	-	V	
Power supply current	I_A	AVCC3	-	1.5	2.1	mA	3 units operating
	I_{AH}		-	-	25	µA	3 units operating *2
	I_R	AVRH1, AVRH2, AVRH3	-	3	6	mA	3 units operating
	I_{RH}		-	-	4.8	µA	3 units operating *2
Variation between channels	-	AN0 to AN23	-	-	4	LSB	

*1: Time for each channel.

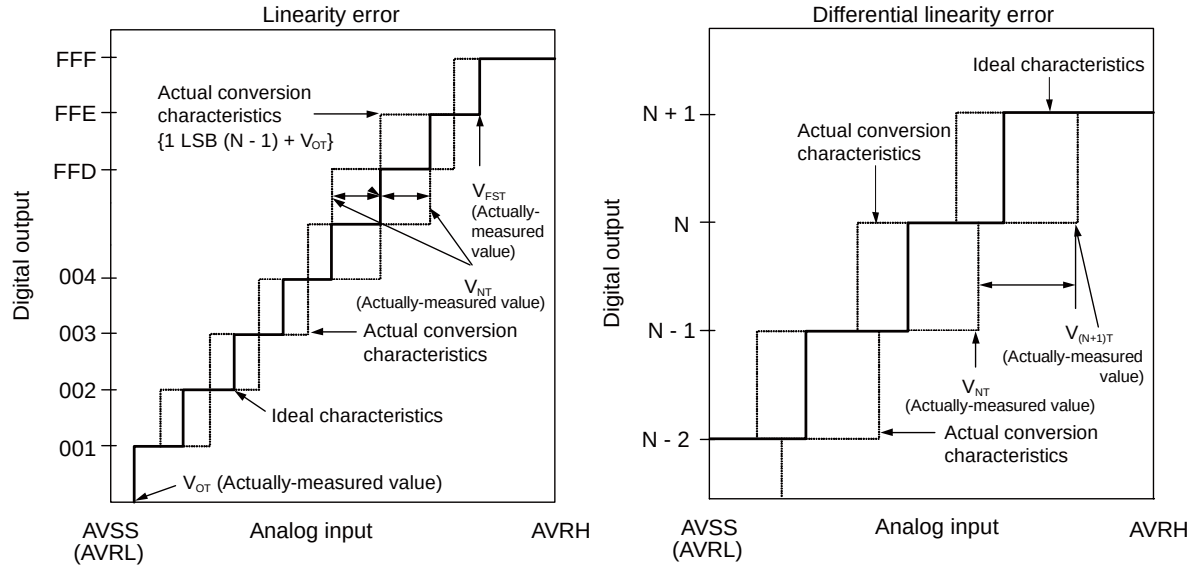
*2: The power supply current (Vcc=AVcc=5.0V) is specified if the A/D converter is not operating and CPU is stopped.

12.5.2 Definition of Terms

Resolution: Analog variation that is recognized by an A/D converter.

Linearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("0000 0000 0000"←→"0000 0000 0001") to the full-scale transition point ("1111 1111 1110"←→"1111 1111 1111").

Differential linearity error: Deviation of the input voltage from the ideal value that is required to change the output code by 1LSB.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N-1) + V_{OT}\}}{1LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1\ LSB \quad [LSB]$$

$$1LSB = \frac{V_{FST} - V_{OT}}{4094} \quad [V]$$

V_{OT}: Voltage at which the digital output changes from "000 $_H$" to "001$_H$".

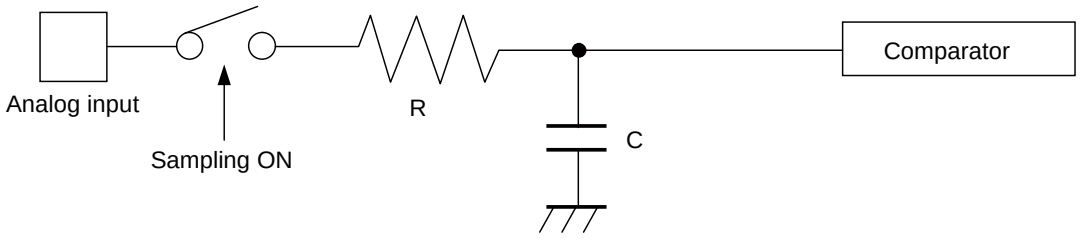
V_{FST}: Voltage at which the digital output changes from "FFE $_H$" to "FFF$_H$".

12.5.3 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 μF) to the analog input pin.

Analog input circuit model



	R	C	
12bit A/D	1.9kΩ (max)	8.30pF (max)	(4.5V≦ Avcc ≦5.5V)

Note: Listed values must be considered as reference values.

12.6 D/A Converter

(T_A: Recommended operating conditions, V_{CC}=AV_{CC}=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Differential linearity error	-	-	-4.0	-	+4.0	LSB	When the analog output voltage is 0.5V to 4.5V

12.7 Flash memory

12.7.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	200	800	ms	8 Kbyte sector[*1] excluding internal preprogramming time
	-	300	1100	ms	8 Kbyte sector[*1] including internal preprogramming time
	-	400	2000	ms	64 Kbyte sector[*1] excluding internal preprogramming time
	-	700	3700	ms	64 Kbyte sector[*1] including internal preprogramming time
8-bit writing time	-	9	288	µs	Excluding overhead time at system level[*1]
16-bit writing time	-	12	384	µs	Excluding overhead time at system level[*1]
ECC writing time	-	9	288	µs	Excluding overhead time at system level[*1]
Erase cycle[*2]/ Data retention time	1,000 cycles/20 years, 10,000 cycles/10 years, 100,000 cycles/5 years	-	-	-	Average temperature T_A=+85°C[*3]

*1: The guaranteed value for erase up to 100,000 cycles

*2: Number of erase cycles for each sector

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

12.7.2 Notes

While the Flash memory is written or erased, shutdown of the external power supply (Vcc) is prohibited.
In the application system where Vcc might disappear while writing, be sure to turn the power off by using an external low-voltage detector.
To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc at 2.7V or more within the duration calculated by the following expression:

Td*[µs] + (period of PCLK [µs] × 257) + 50[µs]

*: See "12.4 AC characteristics 12.4.8 Low-voltage detection (External low-voltage detection)

R/D Converter

(T_A: Recommended operating conditions, V_{CC} = AV_{CC} =5.0V±5%, V_{SS}=AV_{SS}=0.0V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Excitation signal output	Output voltage (amplitude)	$0.4V_{CC}$-1%	$0.4V_{CC}$	$0.4V_{CC}$+1%	V	
	Output voltage (displacement)	-$0.4V_{CC}$+(V_{CC}/2)	-	$0.4V_{CC}$+(V_{CC}/2)	V	
	Output current	-	-	1	mA	
	Frequency	-	10 or 20	-	kHz	Setting with the register
Resolver response signal*1	Amplitude	AREF2-2.0	-	AREF2+2.0	V	
	Maximum input frequency	-	-	24	kHz	
Excitation input signal*2	Amplitude	0	-	AVCC0	V	More than $2V_{p-p}$
	Phase difference from resolver detection signal	-45	-	45	°	
Angle output	Angle accuracy (conversion accuracy)	-4	-	4	LSB	Variation when pausing: ±1LSB
	Resolution	-	12	-	bit	
	Output delay	1.1	-	2.1	µs	
Angular velocity output	Maximum angular velocity	-	-	4000	rps	When bandwidth 1.8kHz mode
		-	-	3000	rps	When bandwidth 600kHz mode
	Resolution	-	0.261	-	rps/LSB	
Reference output voltage	AREF2 output voltage	AVCC0/2-3%	-	AVCC0/2+3%	V	

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Operating characteristics	Tracking loop characteristics (0dB cross frequency)	-	-	1.2	kHz	When bandwidth 1.8kHz mode *3
		-	-	400	Hz	When bandwidth 600Hz mode *3
	Tracking loop characteristics (-3dB cross frequency)	-	-	1.8	kHz	When bandwidth 1.8kHz mode *3
		-	-	600	Hz	When bandwidth 600Hz mode *3
	Maximum tracking rate	-	-	4000	rps	When bandwidth 1.8kHz mode
		-	-	3000	rps	When bandwidth 600Hz mode
	Settling time (179° step).	-	-	4	ms	When bandwidth 1.8kHz mode
		-	-	12	ms	When bandwidth 600Hz mode
	Maximum angular velocity	-	-	1,000,000	rad/s2	When bandwidth 1.8kHz mode
		-	-	150,000	rad/s2	When bandwidth 600Hz mode

*1: Corresponding pin: COS_PLUS,COS_MINUS,SIN_PLUS,SIN_MINUS

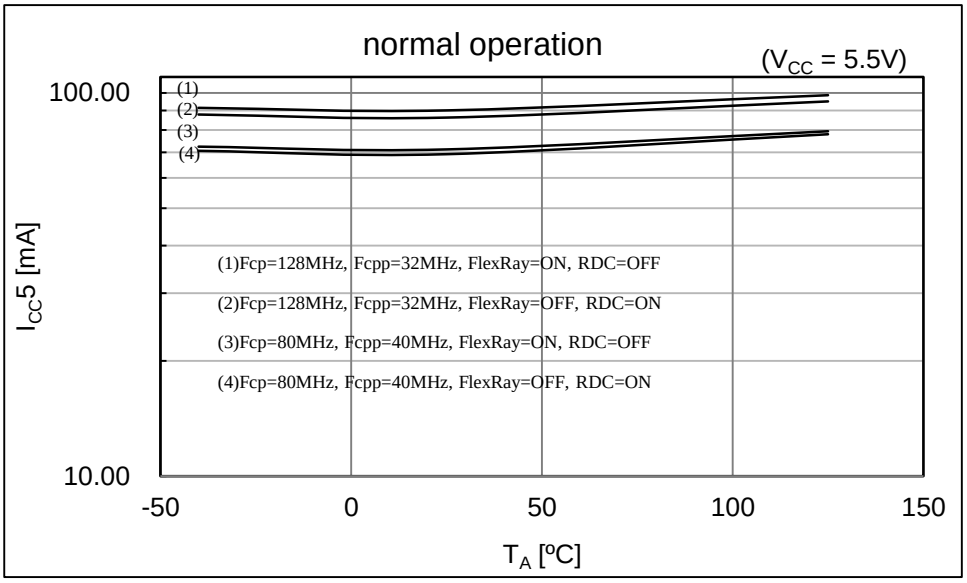
*2: Corresponding pin: MAG_PLUS,MAG_MINUS

*3: When signal amplitude is nominal

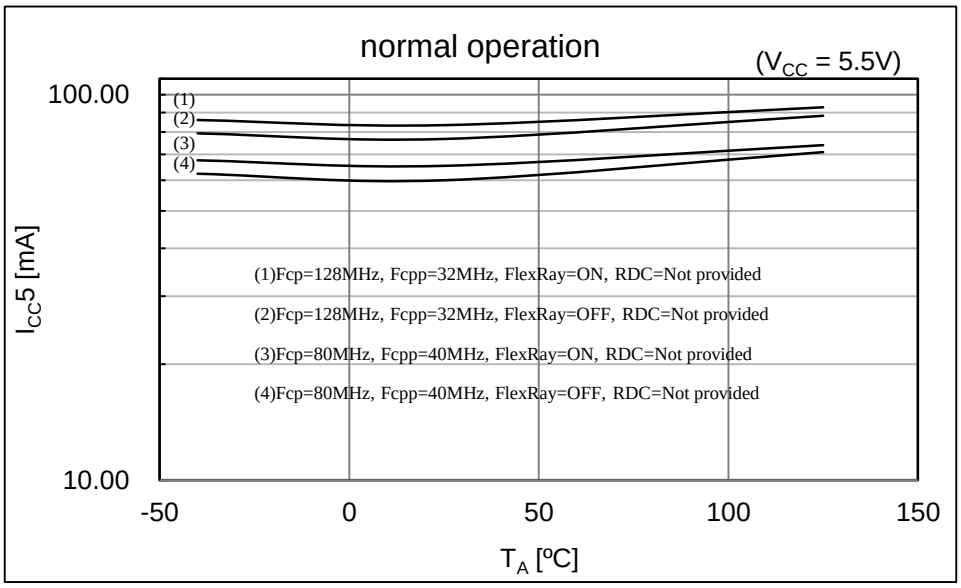
13. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

MB91F585LA/F586LA/F587LA/F585LC/F586LC/F587LC



MB91F585LB/F586LB/F587LB/F585LD/F586LD/F587LD



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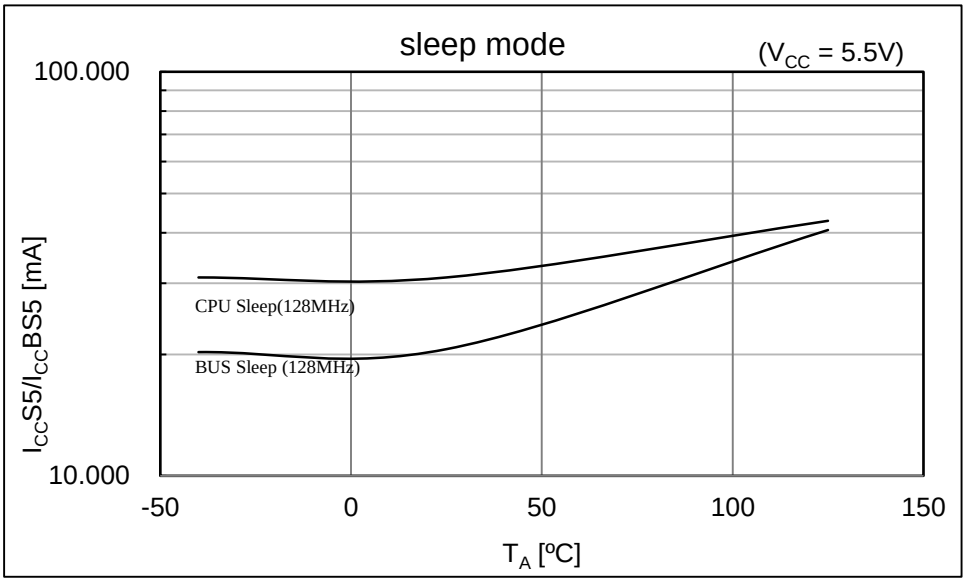

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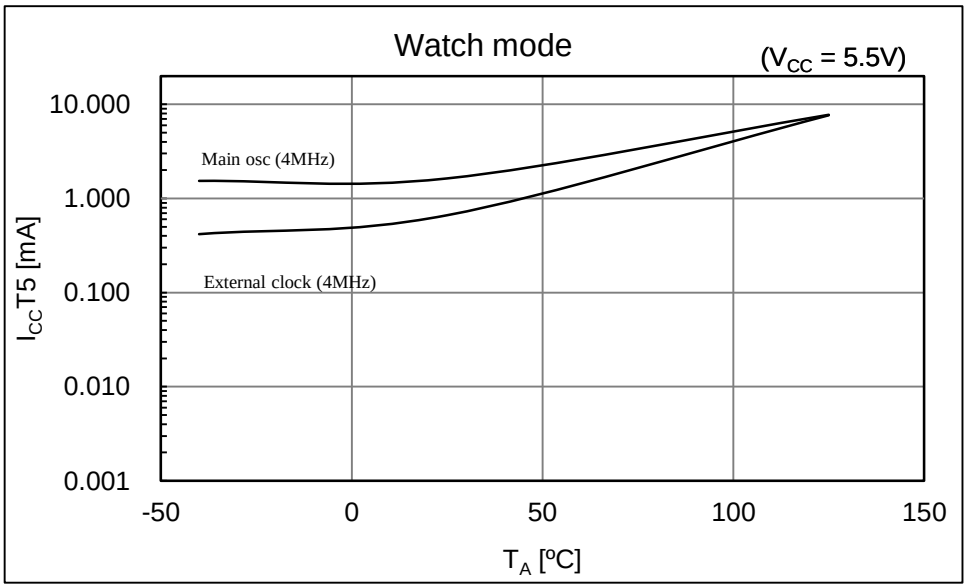

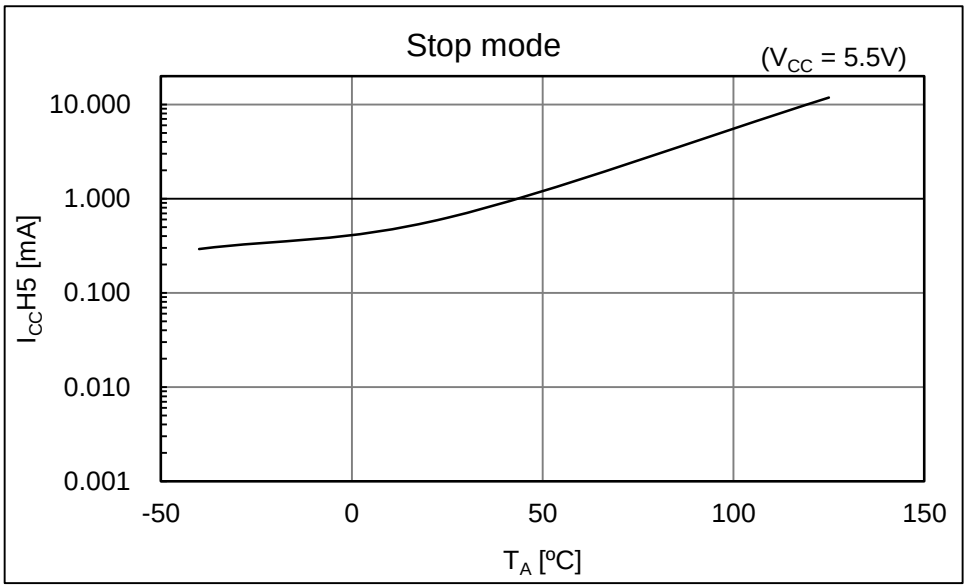

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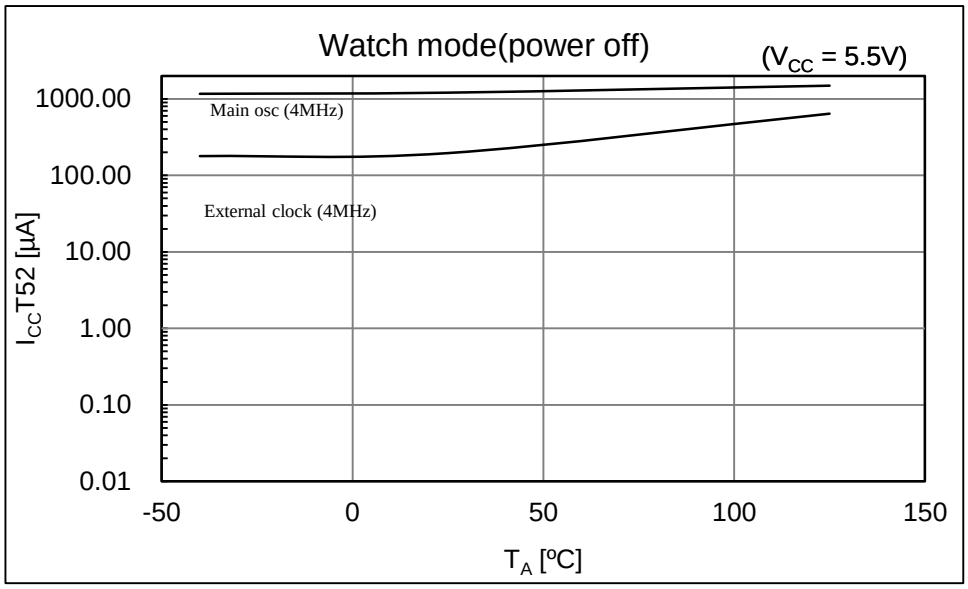
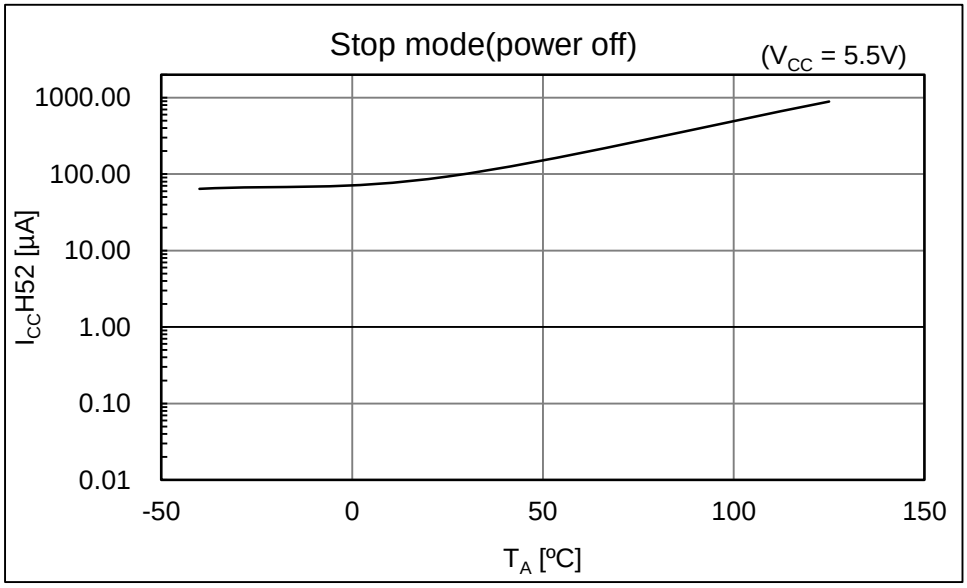
F585LC/F586LC/F587LC/F585LD/F586LD/F587LD





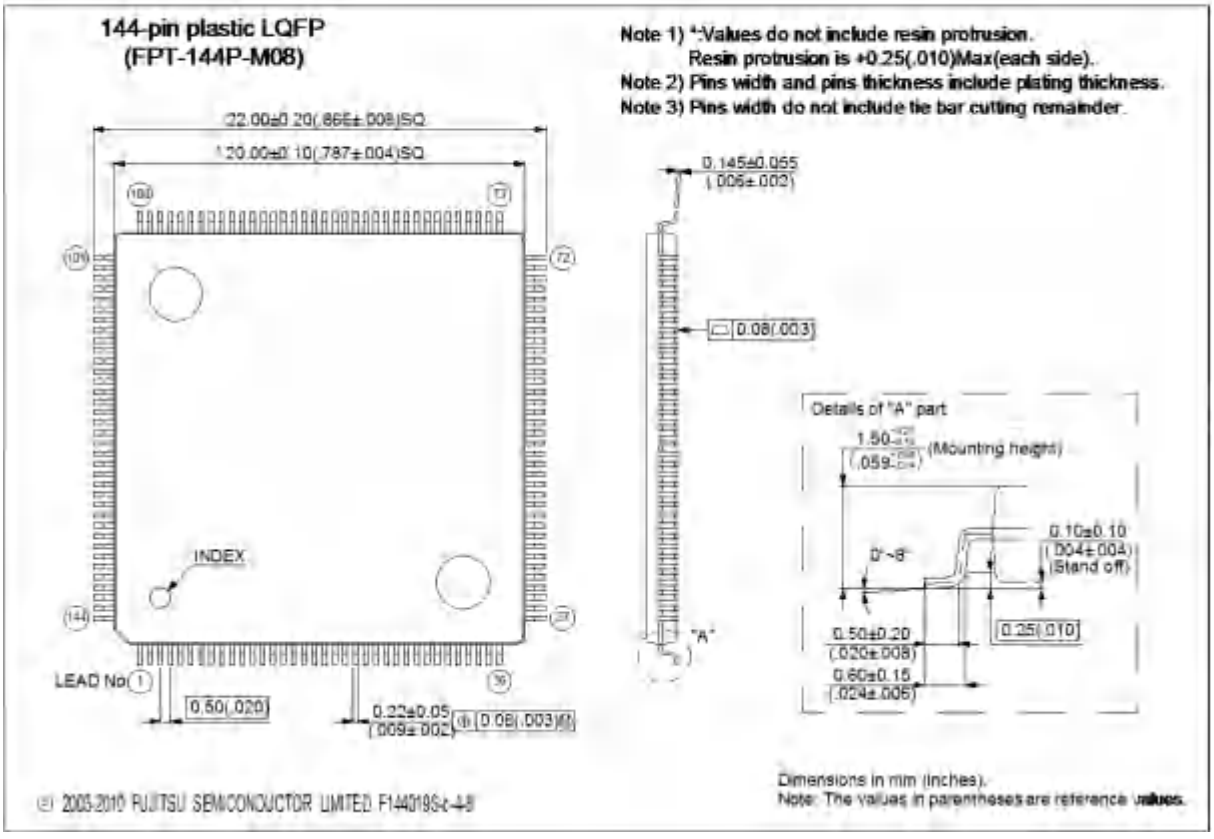
14. Ordering Information

Part number	Package*
MB91F585LAPMC-GTE1 MB91F586LAPMC-GTE1 MB91F587LAPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LBPMC-GTE1 MB91F586LBPMC-GTE1 MB91F587LBPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LCPMC-GTE1 MB91F586LCPMC-GTE1 MB91F587LCPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)
MB91F585LDPMC-GTE1 MB91F586LDPMC-GTE1 MB91F587LDPMC-GTE1	144-pin plastic LQFP (FPT-144P-M08)

*: For details of the package, see " Package Dimensions ".

15. Package Dimensions

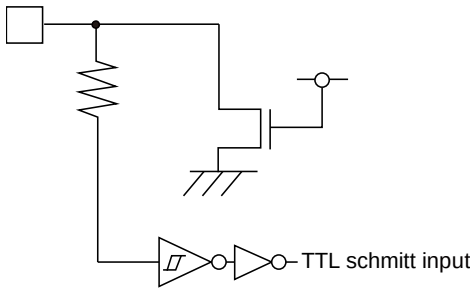
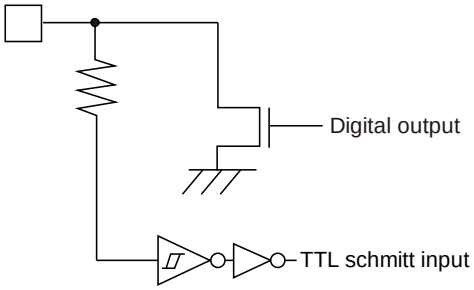
144-pin plastic LQFP		
 (FPT-144P-M08)	Lead pitch	0.50 mm
	Package width × package length	20.0 × 20.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	1.20 g
	Code (Reference)	P-LFQFP144-20×20-0.50



16. Major Changes

Spansion Publication Number: MB91F587LA_DS705-00012

Page	Section	Change Results
Revision 1.0		
-	-	Initial release.
Revision 1.1		
-	-	Company name and layout design change
Revision 2.0		
2	Features	The feature of CR oscillation is corrected. Oscillation frequency: 100kHz, with frequency accuracy ± 10% ↓ Oscillation frequency: 100kHz, with frequency accuracy ± 50% (pre-trimming)
6, 7	Features	The configuration of Waveform generator is corrected. 1 unit (6 channels) + 1 channel ↓ 2 unit (7channels)

Page	Section	Change Results
28	I/O Circuit Type	The figure of type "L" is corrected.  ↓ 
28, 29	I/O Circuit Type	The specification of "H" level input voltage and "L" level input voltage of FlexRay is corrected. FlexRay input (0.65Vcc/0.35Vcc) ↓ FlexRay input (0.7Vcc/0.3Vcc)
39, 40	Memory Map	The memory map is corrected. The address of "Reset vector table" and "Interrupt vector table" are added.
62, 63, 64, 97, 98, 99	I/O map Address: 001504_H,001528_H, $00154C_H$, 001570_H, 001594_H,	The attribution of register is changed. B,H,W ↓ H,W

Page	Section	Change Results
62, 97	I/O Map Address:00150C$_H$	The register name is corrected. STMCR00 → STMCR0
62, 97	I/O Map Address: 00150E$_H$, 001510$_H$, 001511$_H$, 001512$_H$, 001513$_H$	The registers are deleted. SCSCR0, SCSTR30, SCSTR20, SCSTR10, SCSTR00
73, 108	I/O Map Address:00D310$_H$	The initial value of MHDS is corrected. -0000000 -0000000 -0000000 10000000 ↓ -0000000 -0000000 -0000000 00000000
114	Electrical Characteristics Absolute Maximum Ratings	The remark of "Operating temperature" is corrected. *10 ↓ *10, *11
115	Electrical Characteristics Absolute Maximum Ratings	The explanatory note *11 is added. *11: When it is used exceeding T_A=125°C, contact your sales representative.
116	Electrical Characteristics Recommended operating conditions	"Smoothing capacitor" is changed. Smoothing capacitor* ↓ Smoothing capacitor*1
116	Electrical Characteristics Recommended operating conditions	The remark of “Operating temperature” is added. *2
116	Electrical Characteristics Recommended operating conditions	The explanatory note is corrected. *: For connection of smoothing capacitor CS, see the figure below. ↓ *1: For connection of smoothing capacitor CS, see the figure below. *2: When it is used exceeding T_A=125°C, contact your sales representative.
117	Electrical Characteristics DC Characteristics	The specification of "H" level input voltage of P003 - P007, P010 is corrected. Min:0.65 ×Vcc ↓ Min: 0.7 × Vcc

Page	Section	Change Results
118	Electrical Characteristics DC Characteristics	The specification of "L" level input voltage of P003 - P007, P010 is corrected. Max:0.35 ×Vcc ↓ Max: 0.3 × Vcc
124	Electrical Characteristics AC Characteristics Main Clock Timing	The remark of "CAN PLL jitter" is deleted.
124	Electrical Characteristics AC Characteristics Main Clock Timing	The specification of "The Built-in CR oscillation frequency" is corrected. Min: 90kHz, Max: 110kHz ↓ Min:50kHz Max:150kHz,

Page	Section	Change Results
137, 139, 141, 143	Electrical Characteristics AC Characteristics Multi-function Serial CSIO timing (SMR:MD2-0="010"b) When the serial chip select is used (SCSCR:CSEN=1) Serial clock output signal detect level "H" (SMR,SCSFR:SCINV=0) Serial chip select inactive level "H" (SCSCR,SCSFR:CSLVL=1) When the serial chip select is used (SCSCR:CSEN=1) Serial clock output signal detect level "L" (SMR,SCSFR:SCINV=1) Serial chip select inactive level "H" (SCSCR,SCSFR:CSLVL=1) When the serial chip select is used (SCSCR:CSEN=1) Serial clock output signal detect level "H" (SMR,SCSFR:SCINV=0) Serial chip select inactive level "L" (SCSCR,SCSFR:CSLVL=0) When the serial chip select is used (SCSCR:CSEN=1) Serial clock output signal detect level "L" (SMR,SCSFR:SCINV=1) Serial chip select inactive level "L" (SCSCR,SCSFR:CSLVL=0)	The specifications of t_{CSSI}, t_{CSHI} and t_{CSDI} are corrected. ·t_{CSSI} Min: -50-t_{CSSU} *1 Max: +0-t_{CSSU} *1 ↓ Min: t_{CSSU} *1+0 Max: t_{CSSU} *1+50 ·t_{CSHI} Min: +0+t_{CSHD} *2 Max: +50+t_{CSHD} *2 ↓ Min: t_{CSHD} *2-50 Max: t_{CSHD} *2+0 ·t_{CSDI} Min: -50+t_{CSDS} *3 Max: +50+t_{CSDS} *3 ↓ Min: -50+5t_{CPP}+t_{CSDS} *3 Max: +50+5t_{CPP}+t_{CSDS} *3

Page	Section	Change Results
146	Electrical Characteristics AC Characteristics Multi-function Serial I^2C timing (SMR:MD2-0="100"b)	The explanatory note *1 is corrected. *1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. VP shows that the power supply voltage of the pull-up resistor and IOL shows the VOL guarantee current. ↓ *1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. VP shows that the power supply voltage of the pull-up resistor and IOL shows the VOL guarantee current.
162	Electrical Characteristics Flash memory	Item name is changed. (1) Main Flash ↓ (1) Electrical Characteristics
162	Electrical Characteristics Flash memory	The remark of " Erase cycle*2 / Data retention time " is corrected. Temperature at writing/erasing Tj <+105°C Average temperature T_A=+85°C *3 ↓ Average temperature T_A=+85°C *3
164	Electrical Characteristics R/D Converter	The remark of " Amplitude" of "Resolver response signal*1 " is added. More than 2Vp-p
165-168	Example Characteristics	"Example Characteristics" is newly added.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB91F585LA/B/C/D, MB91F586LA/B/C/D, MB91F587LA/B/C/D, FR81S, MB91580L Series Microcontroller Datasheet
Document Number: 002-04663

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	KOJM	08/22/2014	Migrated to Cypress and assigned document number 002-04663. No change to document contents or format.
*A	5137994	KOJM	03/16/2016	Updated to Cypress template

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